Demande n°3880 - ARED

Acronyme :FAMA

Identification

Identification

N°	3880
Année	2025
Statut	Brouillon
Date de création	29/01/2025
Date de modification	29/01/2025
Date de soumission	29/01/2025
Acronyme	FAMA
Intitulé du projet	Fiabilité des Accélérateurs MAtériels à l'ère Post-Von Neumann
Dispositif	ARED

Priorité régionale

Stratégie régionale de recherche et d’innovation (S3)

Stratégie régionale de recherche et d’innovation (S3)

Domaine d'innovation stratégique principal	Économie numérique sécurisée et responsable
Levier thématique associé au DIS principal	Spatial

Organisme de tutelle

Organisme de tutelle

Etablissement	UNIVERSITE RENNES 1
Commune	RENNES
Civilité	Monsieur
Nom	Le Gouguec
Prénom	Fabrice

Unité de recherche

Unité de recherche

Nom de l'unité	IRISA
Civilité	Monsieur
Nom	Guillaume
Prénom	Gravier
Courriel	guig@irisa.fr

Données complémentaires de l'unité de recherche

Libellé	Valeur
Statut et numéro de l'unité de recherche (UMR, USR, EA)	
Le cas échéant, nom de l'équipe de recherche	TARAN
Le cas échéant, nom du responsable de l'équipe de recherche	Olivier Sentieys
Activités de recherche et points forts de l'équipe	L'équipe TARAN développe des architectures matérielles en mettant l'accent sur la fiabilité, l'efficacité énergétique et l'accélération matérielle. Ses travaux portent sur l'intégration hétérogène, l'optimisation des circuits et des interactions entre sécurité, fiabilité et contraintes temporelles.
Si implication dans un/plusieurs programmes européens ou internationaux, préciser	

Co-directeur de thèse

Description

Description du projet

Libellé	Valeur
Résumé synthétique du projet (2000 caractères max)	L'intelligence artificielle (IA) devient indispensable dans divers secteurs en raison de son potentiel à transformer les applications, des maisons intelligentes aux systèmes critiques pour la sécurité, tels que la conduite autonome et l'exploration spatiale. Les deep neural networks (DNN) sont des méthodes d'IA de pointe pour le traitement du langage, la classification d'images et de vidéos, ainsi que le traitement audio et radar [1–3]. Des DNN comme GPT-4 et Mixture of Experts se distinguent par leur haute précision. Pour déployer ces DNN complexes dans des systèmes où la puissance et les performances sont essentielles, de nouvelles architectures d'accélérateurs, telles que celles basées sur le processing in memory (PIM), ont été proposées [4]. Dans des applications critiques telles que l'avionique et l'exploration spatiale, la fiabilité des accélérateurs PIM est une exigence cruciale. Il est donc essentiel de caractériser cette fiabilité afin de mettre en œuvre des techniques de tolérance aux faultes. La caractérisation peut se faire par : 1) la simulation de faultes, qui permet d'identifier des sites spécifiques mais nécessite des modèles de faultes réalistes ; 2) des expériences physiques avec exposition aux radiations, qui offrent des estimations fiables du taux de défaillance, mais limitent l'observation de la propagation des faultes. Dans cette thèse, nous identifierons les vulnérabilités des accélérateurs PIM et leur impact sur les DNN via des simulations de faultes et des expériences de radiation. Nous proposerons ensuite des techniques d'atténuation des faultes adaptées au matériel PIM pour atténuer les défaillances induites par les radiations. 1-Scaling Vision Transformers, CVPR2022 2-Compound fault diagnosis for industrial robots based on dual-

Libellé	Valeur
	2-Compound fault diagnosis for industrial robots based on dual-transformer networks, JMS2023 3-EVA-02: A Visual Representation for Neon Genesis, CVPR2023 4-Roadmap to neuromorphic computing with emerging technologies, APL2024
Caractère structurant/stratégique du projet (descriptif/ex. : art.5 Rglmt ARED 2025 -2000 car. max)	Ce projet s'inscrit pleinement dans l'axe stratégique de l'économie numérique sécurisée et responsable, en développant des architectures de calcul émergentes (accélérateurs PIM et neuromorphiques) adaptées aux systèmes critiques comme le spatial, la défense ou l'intelligence artificielle embarquée. En répondant aux défis de performance, d'efficacité énergétique et de résilience face aux radiations, il renforce l'expertise bretonne en technologies numériques de pointe. Sur le plan académique, le projet bénéficie de l'environnement scientifique du centre Inria Rennes, un acteur clé du numérique en Bretagne. Il s'appuie sur des collaborations internationales (Rutherford Appleton Laboratory au Royaume-Uni, Los Alamos National Laboratory aux États-Unis), permettant au doctorant de se former dans un domaine de pointe et de renforcer le rayonnement scientifique de la région à l'échelle internationale. Enfin, ce projet a un impact industriel et socio-économique important. En améliorant la fiabilité et la sécurité des technologies embarquées, il soutient des secteurs stratégiques régionaux, comme le spatial, la défense et l'industrie 4.0, tout en stimulant des partenariats avec des entreprises locales et nationales.
Porteur du projet : date d'obtention de l'HDR ou dérogation	Angeliki KRITIKAKOU, 28 novembre 2022
Collaborations scientifiques (nature/pays) et partenariat socio-économique envisagé (3000 car. max.)	Ce programme de doctorat traitera des défis de fiabilité liés aux technologies émergentes, en particulier les accélérateurs matériels PIM pour les DNN. Nous prévoyons de développer plusieurs collaborations scientifiques avec des entreprises et des universités. Actuellement, nous collaborons avec UPMEM en France et STMicroelectronics en Italie dans le cadre du projet européen ARCHYTAS. UPMEM est spécialisé dans les accélérateurs PIM, tandis que STMicroelectronics est un leader de l'industrie des semi-conducteurs, également très présent dans les marchés critiques pour la sécurité et les missions spatiales. De plus, nous envisageons des collaborations potentielles avec Sorbonne Université (France), avec lesquelles nous avons déjà établi des partenariats de recherche à long terme.
Si DIS identifié, préciser l'adéquation du projet avec le DIS (2000 car. maximum)	Le projet de thèse Fiabilité des Accélérateurs Matériels à l'ère post-Von Neumann s'inscrit dans le Domaine d'Innovation Stratégique (DIS) de l'économie numérique sécurisée et responsable, et en particulier sur le secteur spatial, un levier stratégique pour la Bretagne. Ce projet explore des architectures de calcul émergentes, comme les accélérateurs PIM, adaptées aux systèmes critiques tels que les applications spatiales. Ces technologies permettent de déployer des modèles complexes d'intelligence artificielle (IA) dans des environnements contraints en énergie, comme les satellites et autres infrastructures spatiales. Elles offrent une alternative économe en énergie aux GPU et TPU classiques, en réponse aux besoins croissants d'optimisation des performances et de durabilité dans le secteur spatial. Ces avancées s'inscrivent directement dans les priorités du DIS, en renforçant la sécurité, l'efficacité et la fiabilité des technologies numériques. Dans le contexte spatial, la résilience des systèmes embarqués est essentielle, notamment face aux radiations présentes dans l'espace, qui peuvent entraîner des fautes critiques. Ce projet propose de caractériser les vulnérabilités matérielles et logicielles des architectures PIM et de développer des solutions de durcissement pour garantir leur robustesse. Porté par le centre Inria Rennes et s'appuyant sur un écosystème local d'excellence en numérique et spatial, le projet bénéficie de collaborations internationales de premier plan. Il renforce le rayonnement scientifique et technologique de la Bretagne en positionnant la région comme un acteur clé de l'innovation numérique appliquée au spatial.
Si priorité régionale cochée, préciser en quoi le projet s'y rattache effectivement (2000 car.max.)	Le projet s'aligne étroitement sur la priorité régionale de la cybersécurité. En explorant la fiabilité des architectures de calcul non conventionnelles (PIM, neuromorphiques) face aux fautes induites par les radiations, il contribue à garantir la sécurité et la résilience des systèmes critiques. Ces travaux

	répondent aux besoins régionaux et nationaux en matière de protection des infrastructures numériques stratégiques (défense, spatial, IA embarquée).
Si priorité régionale "Politique publique Région", préciser (voir liste au point 4, Règlement 2025)	Le projet s'aligne étroitement sur la priorité régionale de la cybersécurité. En explorant la fiabilité des architectures de calcul non conventionnelles (PIM, neuromorphiques) face aux fautes induites par les radiations, il contribue à garantir la sécurité et la résilience des systèmes critiques. Ces travaux répondent aux besoins régionaux et nationaux en matière de protection des infrastructures numériques stratégiques (défense, spatial, IA embarquée).
Cotutelle financière internationale (oui/non)	Non
Nom(s) du(des) cofinanceur(s) envisagé(s) ou confirmé(s)	European Project (EDF) - ARCHYTAS - 24CE310-02D
Si cofinancement industriel, justifier le choix du dispositif ARED au lieu du dispositif CIFRE	
État du cofinancement (indiquer "acquis" ou "demandé")	Acquis
Si demandé, date prévisionnelle de réponse du cofinanceur	
Si cofinancement refusé, autre(s) source(s) de cofinancement identifiée(s)	
Si reversement prévu, préciser (partenaire, montant)	

Candidat

Collaboration internationale

Collaboration internationale

Pays	
Etablissement partenaire à l'étranger	

Pièces jointes

Date de mi	Type de pièce	Commentaire	Document	Valide	Commentaire
29/01/2025	ARED - Dépôt - CV du porteur	Obligatoire - Le CV doit préciser si le porteur est titulaire de l'HDR et, le cas échéant, depuis quand, et mentionner la liste des doctorant·e·s déjà encadré·e·s et des publications associées.	Long_CV_english-4.pdf	Non traité	
	ARED - Dépôt - Avis directeur·rice d'unité	Obligatoire - Voir le modèle à suivre dans l'onglet "Documents à télécharger"		Non traité	
	ARED - Dépôt - Justificatif cofinancement	Facultatif - Dépôt de demande, justificatif d'obtention, courrier du cofinanceur pressenti...		Non traité	
	ARED - Dépôt - Lettre partenaire étranger	Facultatif - Lettre d'engagement de l'établissement partenaire étranger en cas de cotutelle internationale		Non traité	

	ARED - Dépôt - Pièce complémentaire	Facultatif		Non traité	
	ARED - Dépôt - Pièce complémentaire	Facultatif		Non traité	
	ARED - Instruction - Lettre de saisine	Lettre de l'établissement à transmettre à la Région (utiliser le modèle disponible dans la rubrique "Documents à télécharger")		Non traité	
	ARED - Versement - Convention de partenariat	Le cas échéant (si autorisation de reversement)		Non traité	
	ARED - Versement 2 - CV doctorant.e	Pour versement tranche 2		Non traité	
	ARED - Versement 2 - Copie du contrat doctoral (ou CDD ou attestation))	Pour versement tranche 2		Non traité	
	ARED - Versement 2 - Attestation bon déroulement travaux année 1	Pour versement tranche 2		Non traité	
	ARED - Versement 2 - Bilan financier année 1	Pour versement tranche 2 ARED		Non traité	
	ARED - Versement 3 - Attestation bon déroulement travaux année 2	Pour versement 50% tranche 3 ARED		Non traité	
	ARED - Versement 3 - Bilan financier année 2	Pour versement 50% tranche 3 ARED		Non traité	
	ARED - Versement 4 - Bilan financier année 3	Pour versement solde année 3 ARED		Non traité	
	ARED - Versement 4 - Certificat administratif précisant statut thèse	Pour versement du solde de la tranche 3		Non traité	

Curriculum Vitae (CV)

Angeliki KRITIKAKOU

Maître de conférences à l'Université de Rennes
et
Chair d'Innovation à l'Intitut Universitaire de France (IUF)

Equipe TARAN - Univ Rennes, IRISA, Inria, CNRS

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1 Personal information

Name Surname	Angeliki KRITIKAKOU
Position	Associate professor (HDR)[1] and Chair of Innovation[2]
Affiliation[1]	Dep. Computer science and electronics ISTIC - UFR 6074 University of Rennes
Team	TARAN
Address	Campus Beaulieu 263 Avenue du General Leclerc 35000, Rennes, France
Affiliation[2]	Institute Universitaire de France (IUF), France
Telephone	+33 2 99 84 71 00, +33 7 81 86 60 89
E-mail	angeliki.kritikakou@irisa.fr
Site web	www.people.rennes.inria.fr/angeliki.kritikakou
Nationality	Greek, French
Birth date	12 April 1983
Gender	Feminine



2 Summary

Career

- **Chair of Innovation**, Junior member, Institute Universitaire de France (IUF), France (10/2023 - 09/2028)
- **Associate professor** (Since 09/2014) with **HDR in Computer Science** (11/2022)
  - Research activities: Institute for Research in IT and Random Systems (IRISA)/INRIA Center at Rennes University, France
  - Teaching activities: Dep. Computer Science & Electronics (ISTIC), University of Rennes, France
- **Post-doctoral researcher** (09/2013 - 08/2014)
  - Research activities: Dep. Modeling & Information Processing Department (DTIM) of French Aeronautics & Space Research Center (ONERA) in collaboration with the Laboratory of Analysis & Architecture of systems (LAAS) and Institute of Computer Science of Toulouse (IRIT), Toulouse, France
  - Teaching activities: Teaching assistant at Dep. Networks & Telecommunications, Superior National School of Electronics, Electrical engineering, Computer science, Hydraulics and Telecommunications (ENSEEIHT), Institute National Polytechnic (INP) of Toulouse, France (01/2014 - 06/2014)
- **Post-doctoral researcher** (06/2013 - 08/2013)
  - Research activities: Dep. Electrical and Computer Engineering (ECE), School of Engineering, University of Patras, Greece
- **PhD in Electrical and Computer Engineering** (03/2009 - 05/2013)
  - Research activities: Dep. Electrical and Computer Engineering (ECE), School of Engineering, University of Patras, Greece, in collaboration with the research institute Inter-university Microelectronics Center (IMEC), Leuven, Belgium
  - Teaching activities:
    - Teaching assistant at Dep. Electrical & Computer Engineering (ECE), School of Engineering, University of Patras, Greece (09/2011 - 08/2012)

    - Non-tenured lecturer (09/2010 - 08/2011) at:
        - Technological Educational Institute of Patras (TEI), Greece
        - Public Institute of Vocational Training of Patras (IEK), Greece
        - Dep. Electrical & Computer Engineering (ECE), School of Engineering, University of Patras, Greece
- **Master of Science (MSc)** in "Integrated Software and Hardware Systems", Dep. Computer Engineering & Informatics (CEID), School of Engineering, University of Patras, Greece (09/2007 - 03/2009)
  – **Teaching assistant** at Dep. Computer Engineering & Informatics (CEID), School of Engineering, University of Patras, Greece (09/2007 - 08/2008)
- **Diploma (5-year MEng)** at Dep. Electrical and Computer Engineering (ECE), School of Engineering, University of Patras, Greece (Mai 2007)

Teaching activities

Keywords : Computer Architecture, Programming Languages, Operating Systems, Electronics.

Main service to the academic community and responsibilities

Type	**Quantity**
International	
Erasmus+ contact person	**1**
University of Turin (IT) and currently discussions with other EU universities	
National	
French civil service public education system (Agrégation) examination committee	**4**
Industrial Engineering Sciences and Computer Engineering (SII) ('22, '23, '24, '25)	
Ministry-assigned member in the French National Council of Universities (CNU)	**6**
CNU 27 ('22, '23, '24, '25, '26, '27)	
Selection committee for associate professor position	**10**
Polytechnic University Hauts-de-France (CNU 27 - 2023, 2022), INSA Rennes (CNU 63 - 2023), University Paris 8 (CNU 27 - 2023), INP Bordeaux (CNU 61 & 63 - 2023), INSA Toulouse (CNU 27 & 61 - 2022), CenteleSupelec (CNU 27 & 61 - 2023, 2022, 2021), University of Valenciennes (CNU 27 - 2018)	
Local	
Student admission committee	**5**
L3 computer science, University of Rennes 1 ('18-'22)	
Academic jury	**8**
L3 computer science, University of Rennes 1 ('17-'24)	
Master co-responsible	**2x5**
M1 and M2 of Integrated Software and Hardware Systems, University of Patras, Greece ('09-'13)	
Course responsible	**9**
Multitasking operating systems, C language and shell scripting, Computer programming, Introduction to Unix, Introduction to Unix, Algorithmic development & Structured programming, Electronics, Technical industrial design & electric schematics, Introduction to computer science, Accounting and spreadsheets	
Web site developer and administrator	**4**
Master Integrated Software and Hardware Systems, Nanoelectronics network, Dep. Electrical and Computer Engineering, TARAN team	
Local Board of European Students of Technology (BEST)	**4**
University of Patras, Greece (2005-2007)	
Books related to teaching	**2**
Digital Electronics with HSpice, Electrotechnics in practise	

Teaching hours: Tenured position

	2014-15	**2015-16**	**2016-17**	**2017-18**	**2018-19**	**2019-20**	**2020-21**	**2021-22**	**2022-23**	**2023-24**	**2024-25**
Total hours/year	202h	235h	235h	305h	230h	204h	200h	200h	206h	199.5h	199.5h
Discharge hours	96h					128h		32h	64h	128h	128h
Discharge reason	Recr.	-	-	-	-	ERC,CRCT	-	ANR JCJC	ANR JCJC	IUF	IUF

Total hours	**2,416 h**
Average/year	**220 h/year**

Teaching hours: Non-tenured position

	2007-08	**2009-10**	**2010-11**	**2013-14**
Total hours/year	182h	33h	368h	16h

Total hours	**599 h**
Average/year	**150 h/year**

Research activities

Keywords : Dependability, Reliability, Safety, Energy Efficiency, Embedded systems, Computer architecture, Design Space Exploration, Optimisation, Run-time adaptation, Protection and Control Mechanisms.

Publications ([1]Depends on the year)

Type		**Since 2010**
Patent (EP-US)		**1**
Scientific Books (Springer)		**2**
Book chapters		**2**
International journals		**34**
SJR	Q1	15
	TCAS-II, TOSN, JSA, 2xTCAD, 3xJIOT, 2xCS, TETC, TII, JETCAS, TSP, TR	
	Q2	11
	2xTODAES, 3xTNS, P2PNA, TCAD, 3xJS, TACO[1]	
	Q3	8
	MICPRO, IJPP, 2xTODAES, JSPS, 2xJS, TACO[1]	
	Q4	1
	COMLAN	
Int. conf. with proceedings		**51**
Qualis	A1	11
	2xDAC, 6xDATE, 2xRTSS, DSN-S	
	A2	9
	3xECRTS, RTAS, 2xICCD, EMSOFT, VTS, CASES	
	B1	12
	2xISVLSI, 2xETFA, 2xDFT, 5xIOLTS, AdHoc-Now	
	B2	4
	2xETS, 2xSAMOS	
	B3	6
	ICIT, 4xRADECS, VLSI-SoC	
	B4	4
	NANOARCH, NEWCAS, SASP, SECRYPT	
	-	5
	RTNS, CARS, DASIP, Aerospace, EDHPC	
Int. conf. without proceedings		**16**
National conferences		**7**

Student supervision

Post-doctoral	**5**
PhD	**7 + 1**
3 x Current, 4 x Defended, 1 x Abandon	
Internships	**17**
9 x B, 8 x M	

Research Projects

International	**6**
1 x EDF (WP leader), 2 x FP7 1 x ENIAC/ARTEMIS, 1 x H2020 1 x Leonardo da Vinci	
Submitted	1 (MSCA: WP Leader)
National	**7**
1 x ANR JCJC (PI), 1 x ANR PRCE 1 x DGA/RAPID, 1 x Regional 1 x PEPR, 1 x ESIF/CORALLIA 1 x BPI France	
Submitted	2 (AP ASIC: WP Leader, PI)

Research contracts

National	4
1 x Industrial, 3 x Univ. Rennes 1 (PI)	

Main service to research community

Type	**International**	**National**
Phd defense committee (*PhD reporter)	**8**	**12**
1xCY (KIOS), 1xIT (Scuola Superiore Sant'Anna*), 2xSW (Halmstad Univ., Uppsala Univ.), 2xGR (Univ. Patras), 2xIT (Univ. Bologna, Politecnico Torino) 12xFR (ONERA, Univ. Toulouse*, ECL*, Univ. Nantes*, INSA Toulouse*, ISAE-SUPAERO* Sorbonne Univ.*, ENS Paris, Univ. Toulouse, 3xUniv. Rennes)		
PhD advisory committee	**-**	**5**
5xFR (2xINSA Rennes, Sorbonne Univ., 2xUniv. Rennes)		
PhD fellowship jury	**-**	**7**
CORDIS Inria ('15,'16,'17,'18,'19), MI Inria ('20,'21)		
Conference organisation	**22**	**2**
ECRTS'25, RTNS'25, ESWEEK ('25,'24), DDECS'25, IOLTS ('25,'24,'23), DATE ('25), RTSS'23, SELSE'23, ETS ('25,'24,'23), RTAS ('23,'22), ARC'21, ECRTS ('22,'21), ISVLSI ('25,'22,'20), INRIA-SD'22, TORRENTS'13		
Journal editor	**6**	**-**
Elsevier MICROP, Elsevier Journal System Architecture, SI: Elsevier JPDC, Elsevier MICROP, Wiley SPE, CSEE JPES		
Technical Program Committees	**66**	**4**
DAC ('25, '24, outstanding TPC member award), DAC-LBR ('24), RTSS ('23,'22,'21), DATE ('24,'23,'22,'21,'20), EMSOFT ('24,'23), EMSOFT-LBR ('24), CASES'24, ECRTS ('25,'23,'22,'21,'20,'19), RTAS ('25,'24,'23,'21,'20,'19), RTCSA ('25, '24,'23), VLSID ('25), ISVLSI ('25, '24,'23,'22), ETS ('25, '24,'23), ICPADS'23, DS-RT ('24,'23,'22), SAMOS ('24,'23,'22,'21,'20,'19), HPCC ('21,'20), IISWC'20, NPC'22, LATS'25, AEiC'25, ARC ('24,'23,'22,'21), CPSCom ('22,'21), RTNS ('23,'22), SELSE'23, AI-TREATS'24, OSPERT'25, JRWRTC'16, COMPAS ('24,'23,'22,'21)		
Conference Jury	**2**	**-**
ITC'24 (Academic jury of McCluskey Doctoral Thesis Award), DATE'24 (University Fair Award)		
Conference session chairing	**15**	**1**
TPTR'24, RTSS'23, ECRTS'23, ETS ('24,'23), IOLTS ('24,'23,'22), ISVLSI'22 RTAS'22, DATE ('24,'22), SELSE ('23,'22), ARC'21, JSI'22		
Journal review	**26**	**-**
IEEE TC (since 2011), IEEE TVLSI (since 2015), IEEE TCAD (since 2018), IEEE TSUSC (since 2021) IEEE TPDS (since 2023), IEEE TETC (since 2016), IEEE Access (since 2017), IEEE TASE (since 2020), IEEE TNSM (since 2021), IEEE JIOT (since 2019), IEEE TII (since 2022), IEEE D&T (2024), ACM TODAES (since 2019), CSR (since 2024), ACM JETC (since 2021), ACM TECS (since 2021), ACM CS (since 2023), Elsevier JKSUCIS (since 2019), Elsevier COSREV (since 2024), Elsevier MICRO (since 2019), Elsevier JSS (since 2020), Elsevier CN (since 2022), Springer RTS (since 2022), JRR (since 2023), Hindawi MIS (since 2020), Wiley SEP (since 2019), Wiley SPE (since 2019)		
Additional external conference review	**12**	**-**
ICCAD ('22,'21), DAC ('20, '19), FPL'15, CF'18, IECON'15, PATMOS ('13,'12,'11,'10,'09)		
Invited talks	**3**	**2**
Research group animator	**-**	**5**
GDR SOC2 ('22,'23,'24,'25,'26)		

3 Career

Professional carreer & education

10/2023 - now	**Chair of Innovation**, Junior member Institute Universitaire de France (IUF), France
09/2014 - now	**Associate professor (HDR) in Computer Science**
Research	Laboratory IRISA - Inria Rennes Bretagne Atlantique, Team TARAN
Teaching	Dep. Computer Science and Electronics (ISTIC) University of Rennes Rennes, France
HDR	**Habilitation to supervise research** in Computer Science (11/2022) MathSTIC, University of Rennes 1 Rennes, France Title: "Real-time and reliable design of safety-critical embedded systems"
Mobility	Leave for Research or Thematic Conversions (CRCT) (01/2020 - 06/2020) Virtual (COVID'19) Title: "Design space exploration Approaches for Reliable Embedded systems"
09/2013 - 08/2014	**Post-doctoral researcher**
Research	Modeling and Information Processing Department (DTIM) French Aeronautics and Space Research Center (ONERA) Laboratory of Analysis and Architecture of systems (LAAS) Institute of Computer Science of Toulouse (IRIT) Toulouse, France Title: "Run-time control for mixed -critical systems on multicores"
Teaching	**Teaching assistant** (01/2014 - 06/2014) Dep. of Networks and Telecommunications Superior National School of Electronics, Electrical engineering, Computer science, Hydraulics and Telecommunications (ENSEEIHT), Institute National Polytechnic (INP) Toulouse, France
06/2013 - 08/2013	**Post-doctoral researcher**
Research	Dep. Electrical and Computer Engineering (ECE) School of Engineering, University of Patras Patras, Greece Title: "Development of methodologies for memory management and design space exploration of SW/HW computer architectures for designing embedded systems"
03/2009 - 05/2013	**Ph.D in Electrical and Computer Engineering**
Research	Dep. Electrical and Computer Engineering (ECE) School of Engineering, University of Patras Patras, Greece Grade: Excellent Title: "Development of methodologies for memory management and design space exploration of SW/HW computer architectures for designing embedded systems"
Teaching	**Teaching assistant** (09/2011 - 08/2012) Dep. Electrical and Computer Engineering (ECE) School of Engineering, University of Patras Patras, Greece **Non-tenured lecturer** (09/2010 - 08/2011)

	i. Technological Educational Institute of Patras (TEI) ii. Public Institute of Vocational Training of Patras (VINT) iii. Dep. Electrical and Computer Engineering (ECE), School of Engineering, University of Patras Patras, Greece
09/2007 - 03/2009	**Master of Science (MSc)** in "Integrated Software and Hardware Systems" Dep. Computer Engineering & Informatics (CEID) School of Engineering, University of Patras Patras, Greece Grade: 9.67/10 (1st ranked)
Teaching	**Teaching assistant** (09/2007 - 08/2008) Dep. Computer Engineering & Informatics (CEID) School of Engineering, University of Patras Patras, Greece
Mobility	Master Internship (08/2008 - 02/2009) Inter-university Microelectronics Center (IMEC) Dep. Biosystems, KULeuven Leuven, Belgium Holst Centre Eindhoven, The Netherlands Title: "Low cost low energy embedded processor for online biotechnology monitoring applications"
09/2001 - 05/2007	**Diploma of engineer in Electrical and Computer Engineering** Dep. Electrical and Computer Engineering (ECE) School of Engineering, University of Patras Patras, Greece Grade: 8.22/10 (1st ranked) Master: "Computer and electronics" Master internship (09/2006 - 02/2007) Laboratory Applied Electronics, ECE Patras, Greece Title: "Parallel processing in multithreaded environments"
Mobility	Erasmus (02/2006 - 07/2006) Dep. Applied Informatics School of Engineering, University of Valencia Valencia, Spain

Fellowships and awards

2023 - 2028	Research Award from Institute Universitaire de France (IUF) (EUR 5 000/year)
2019 - 2023	Research Award from French Ministry of Higher education and research (PEDR) (EUR 5 000/year)
09/2011 - 03/2013	PhD Fellowship, Public Welfare Foundation Propondis, Piraeus, Greece (EUR 9 600)
03/2009	Award from University of Patras for academic excellence in the Master of Science "Integrated Software and Hardware Systems", Dep. Computer Engineering and Informatics (CEID), University of Patras, Greece (EUR 1 500)
05/2007	Award from University of Patras for ranking first in the Dep. Electrical and Computer Engineering (ECE), University of Patras, Greece

09/2002 - 08/2004	Award from the Greek Ministry of National Education for academic excellence in the academic years (2002-03, 2003-04, 2004-05) in the Dep. Electrical and Computer Engineering (ECE), University of Patras, Greece (EUR 1000 per year)
09/1995 - 08/2001	Award from the Greek Ministry of National Education for academic excellence in the academic years (1995-96, 1996-97, 1998-99, 1999-2000, 2000-2001)

Continuous learning

03/2023	"Constructing your carrier", CNRS INS2I, (2 days, Paris, France)
01/2023	"Learning life-saving techniques", Union of Firemen of Ille et Vilaine, (0.5 days, Rennes, France)
10/2021	"Preparation and support for the supervision of doctoral students", University of Rennes 1 (0.5 days, Rennes, France)
01/2021	"Harassment awareness", INRIA Bretagne Atlantique (0.5 days, Rennes, France)
11/2018	"Learn to read fast", INRIA Bretagne Atlantique (2 days, Rennes, France)
09/2017	"Designing Cyber-Physical Systems - From concepts to implementation: Multi-objective methodologies and tools for self-healing and adaptive systems", Summer School (3 days, Alghero, Italy)
01/2017	"System design based on FPGA Zynq and the developing environment SdSoC", University of Pierre and Marie Curie, Paris, France (2 days, Paris, France)
12/2016	"Tutorial on GPGPU and Parallel programing", INRIA Bretagne Atlantique (1 day, Rennes, France)
09/2016	"Supervise a PhD student", INRIA Bretagne Atlantique (2 days, Rennes, France)
10/2008	"Convert MATLAB to efficient C-code", MathWorks (2 days, Leuven, Belgium)

Languages

Greek	Mother tongue
English	Proficient User (C2)
	University of Michigan, Certificate of Proficiency in English, March 2001
	University of Cambridge, Certificate in Advanced English, December 1999
	University of Cambridge, First Certificate in English, June 1996
French	Proficient User (C2)
Spanish	Independent User (B2)
	Instituto de Cervantes, Certificado Basico, November 2006
German	Independent User (B1)
	Goethe Institut, Zertifikat Deutch, June 2004
Chinese	Elementary User (A1)

4 Teaching activities

Since September 2014, I have a tenured-track position in ISTIC, University of Rennes, France, where I do the majority of my teaching duties. Other institutes where I participate in teaching activities as a tenured-track associate professor are the National Institute of Applied Sciences (INSA) of Rennes and the Université Félix Houphouët-Boigny (UFHB) in Ivory Coast. Prior to my recruitment, I had already teaching experience in several non-tenured positions in ENSEEIHT in France, and ECE, TEI, VINT, and CEID in University of Patras in Greece, for similar activities.

4.1 Service to the academic community and responsibilities

During my carrier, I have several academic responsibilities at international, national and local level.

At international level, I am the contact person for the Erasmus+ bilateral inter-institutional agreement between University of Rennes and University of Turin in Italy (under evaluation). Currently, I am having several on-going discussions with University of Trento in Italy, University of Cyprus, University of Patras, University of Athens and Aristotle University of Thessaloniki in Greece.

At the national level, I am a member of the examination committee of "agrégation" for Industrial Engineering Sciences and Computer Engineering (SII) in the Computer Science option, for a four-year period (2022-2025). This position entails several responsibilities, including the preparation and correction of written examination, the preparation of exercise labs and the evaluation of candidates during oral examinations, the participation in discussions to establish the standards for evaluation, including defining criteria for grading written and oral examinations, setting passing thresholds, and maintaining consistency in evaluation methods. On average, we are receiving on average 80 candidates/year in the written evaluation and the oral examination takes 10 full days/year. Furthermore, I am in my second mandate as a member of the CNU in section 27 (since 2022), which plays a crucial role in ensuring the quality and integrity of higher education and research in France. The members of the CNU have several responsibilities, including the evaluation of academic candidates by assessing the qualifications and academic achievements of candidates applying for academic positions, promotions, and grants, and advocating for the interests and concerns of faculty members, researchers, and students at the national level, as the CNU members serve as representatives of the academic community. Furthermore, I have participated in ten selection committees for associate professor positions as an expert in my domain (CNU sections 27, 61, and 63).

At the local level during my tenure track position, I have been a member of the student admission committee of the 3^{rd} year Bachelor (B3) in computer science, ISTIC, University of Rennes 1 for a four year period (2018-2021), with on average 500 applications to treat over 3 days. Since 2017, I have been a member of the academic jury of the 3^{rd} year Bachelor (B3) in computer science, ISTIC, University of Rennes 1, with on average 120 students and at least 3 reunions per year. Regarding course responsibilities, I have been responsible for the course “Multitasking Operating Systems” taught in English in the first year of masters (M1) for the international master “EIT Digital Cloud Computing and Services” and of the national master “Software Engineering” for a three year period (2015-2018). I renovated the course, prepared many automated online quizzes ($>$ 50 questions) and created new laboratory projects every year. The ISTIC teaching program was modified in 2017. As a consequence of this modification, I gave up the responsibility of this course, which changed context. In 2017, I created a new course entitled “C language and shell scripting” and later “Tools and programming in C”, taught in English in the third year (B3) computer science, for which I am responsible till now. I created the course, the exercises and the laboratory projects, as well as many automated online quizzes ($>$100 questions). I implemented the infrastructure for the organization and the realization of individual lab exams. Since 2022, I am responsible of the C/Unix course in the Université Félix Houphouët-Boigny (UFHB) in Ivory Coast, where I supervise the local professors who give the courses physically, while I am preparing and correcting the exams (on average 50 students). Since 2023, I am responsible of the course “Computer programming”, taught in French in the third year (B3) of electronics and embedded systems professional bachelor, and of the course “Introduction to Unix” in the third year (B3) of computer methods applied to business management (MIAGE).

Prior to my tenure track position, I was co-responsible for the first (M1) and second (M2) year of Master “Integrated Software and Hardware Systems” in the Department of Computer Engineering and Fundamental Informatics (CEID) in University of Patras in Greece during five years (2009-2013). My mains tasks include student recruitment and admission process, program planning and coordination of the semester courses and the exam sessions, student advising, and other administrative tasks, including the developing and administration of the master’s web page. During my adjunct lecturer position, I was responsible for the teaching of several courses, such as “Algorithmic development and structured programming” (B1), “Electronics” (B2),

"Technical industrial design and electrical schematics" (B1), "Introduction to Computer Science" (B1) and "Accounting and spreadsheet" (B2). I was also a member of the Local Board of European Students of Technology (BEST) on University of Patras (2005-2009), where we sought sponsors and organized events and meetings, such as "Renewable Energies - Oil 5-0" and the 2007 annual meeting of Greek BEST. Regarding academic written material, I was the co-author of two books, which have been created under funds from the Greek Ministry of National Education for enforcing the studies in computer science in University of Patras :

1. A. Kritikakou and D. Tsitsipis, "Digital Electronics with HSpice", Department of Computer Engineering and Informatics, School of Engineering, University of Patras, Greece, 2008
2. A. Kritikakou, A. Nanakos, G. Grigoropoulos and V. Papoutsis, "Electrotechnics in practise", Department of Mechanical Engineering, Technological Educational Institute of Patras, Patras, Greece, 2011

Table 3 summarizes my service to the academic community through participation in academic and examination committees, selection committees for academic positions, student admission, master responsibilities and other administration services.

TABLE 3: Service to the academic community and responsibilities

Type	**Quantity**
International	
Erasmus+ contact person	1
University of Turin (IT) and currently discussions with other EU universities	
National	
French civil service public education system (Agrégation) examination committee	4
Industrial Engineering Sciences and Computer Engineering (SII) ('22, '23, '24, '25). Member of the examination jury: Create the writing and oral exam topics, correction of the written exams (80 candidates/year) and oral examination of the candidates (10 days/year).	
Ministry-assigned member in French National Council of Universities (CNU)	6
National Council of Universities - section 27 ('22, '23, '24, '25, '26, '27) Examination of the applications for the Qualification, Promotion and the Award of Teaching and Research	
Academic position committee	10
Associate professor (MCF 27 & 61), CentraleSupelec, Institute for Research in IT and Random Systems (IRISA), France (2023) Associate professor (MCF 27), Univ Paris 8, Artificial Intelligence and Data Semantics Laboratory (LIASD) France (2023) Associate professor (MCF 63), INSA Rennes, Institute of Electronics and Digital Technologies (IETR), France (2023) Associate professor (MCF 27), Polytechnic University of Hauts-de-France, Laboratory of Industrial and Human Automation control, Mechanical engineering and Computer Science) (LAMIH), France (2023) Associate professor (MCF 61 & 63), IMP Bordeaux, Enseirb-Matmeca, Laboratory from Material to System Integration (IMS), France (2023) Associate professor (MCF 27 & 61), INSA Toulouse, Laboratory for Analysis and Architecture of Systems (LAAS-CNRS), France (2022) Associate professor (MCF 27), Polytechnic University of Hauts-de-France, Laboratory of Industrial and Human Automation control, Mechanical engineering and Computer Science) (LAMIH), France (2022) Associate professor (MCF 27 & 61), CentraleSupelec, Institute for Research in IT and Random Systems (IRISA), France (2022) Associate professor (MCF 27 & 61), CentraleSupelec, Institute for Research in IT and Random Systems (IRISA), France (2021) Associate professor (MCF 27), University of Valenciennes and Hainaut-Cambrésis, Laboratory of Industrial and Human Automation control, Mechanical engineering and Computer Science (LAMIH), France (2018)	

Local	
Student admission committee	4
3^{rd} year Bachelor (B3) in computer science, ISTIC, University of Rennes 1 ('18,'19,'20,'21) (500 applications to treat over 3 days)	
Academic jury	7
3^{rd} year Bachelor (B3) in computer science, ISTIC, University of Rennes 1, France (Since 2017, 120 students, at least 3 reunions per year)	
Master co-responsible	2x5
Master of Science "Integrated Software and Hardware Systems", CEID, University of Patras, Greece Co-responsible of 1^{st} (M1) and 2^{nd} (M2) year of master ('09, '10, '11, '12, '13) (typically 20 students per year, 50 student applications to treat)	
Course responsible	9
ISTIC, University of Rennes 1, France: "Multitasking Operating Systems" in 1^{st} year of international master (M1) "EIT Digital Cloud Computing and Services" and "Software Engineering" (2015 - 2018) "C language and shell scripting", 3^{rd} year Bachelor (B3) in computer science (Since 2018) "Computer programming", 3^{rd} year Bachelor (B3) in electronics and embedded system (Since 2023) "Introduction to Unix", 3^{rd} year Bachelor (B3) in computer methods applied to business management (Since 2023) **TEI, University of Patras, Greece:** "Algorithmic development and structured programming", 1^{st} year Bachelor (B1) in business and information systems planning (2010 - 2011) "Electronics", 2^{nd} year Bachelor (B2) in mechanical engineering (2010 - 2011) "Technical industrial design and electrical schematics", 1^{st} year Bachelor (B1) in electrical engineering (2010 - 2011) "Introduction to Computer Science" 1^{st} year Bachelor (B1) in speech and language (2010 - 2011) **VINT, University of Patras, Greece:** "Accounting and Spreadsheet", 2^{nd} year Bachelor (B2) in administration and financial management (2010 - 2011)	
Web site developer and administrator	4
Master of Science "Integrated Software and Hardware Systems", CEID, University of Patras, Greece (2009 - 2013) Internal network of "Nanoelectronics", University of Patras, Greece (2010 - 2013) Dep. Electrical and Computer Engineering (ECE), University of Patras, Greece (2011 - 2013) TARAN team (2022 - now)	
Local Board of European Students of Technology (BEST)	4
University of Patras, Greece (2005-2007)	

4.2 Teaching topics and hours

Table 1 presents in detail the hours carried out since my tenured position and Table 2 presents in detail the hours carried out in previous non-tenured positions.

TABLE 1: Tenured position: Summary of teaching hours (*: Responsible, +: New course)
(CM: Theory, TD: Exercises, TP: Laboratories, B: Bachelor, M: Master, S: Semester)

Course	Year Sem.	Lang.	Num. students	2014-15	2015-16 2016-17	2017-18	2018-19	2019-20	2020-21	2021-22	2022-23	2023-24 2024-25
Home Institution: ISTIC												

Multitasking Operating Systems (*)	M1 S7	English	CM: 60		CM: 20h	CM: 20h						
C language and shell scripting (*,+)	B3	English	CM: 120 TD: 40 TP: 20			CM: 16h TD: 12h TP: 40h	CM: 16h TD: 12h TP: 40h	CM: 16h TP: 20h	CM: 16h TD: 12h TP: 40h	CM: 16h TD: 12h TP: 40h	CM: 16h TP: 20h	CM: 16,5h
Computer Programming (*)	B3 S5	French	CM: 10									CM: 15h
Introduction to Unix (*)	B3 S5	French	CM: 40									CM: 4,5h
Hardware accelerators for AI	M2 S9	French	TP: 16									TP: 7,5h
Computer architectures 1	B3 S5	French	TD: 40 TP: 20	TD: 18h TP: 32h	TD: 18h TP: 32h							
Computer architectures 2	B3 S6	French	TD: 40 TP: 20		TD: 16h TP: 36h							
Principles of processor operation	B3 S5	French	TD: 40 TP: 20			TD: 8h TP: 24h	TD: 8h TP: 24h	TD: 8h TP: 24h	TD: 8h TP: 24h	TD: 8h TP: 24h	TD: 8h TP: 24h	
Software/Hardware interface	B3 S6	French	TD: 40 TP: 20			TD: 12h TP: 32h	TD: 12h TP: 32h		TD: 12h TP: 32h	TD: 12h	TD: 12h TP: 16h	
Operating Systems 1	B3 S5	French	TP: 20	TP: 24h	TP: 24h							
Operating Systems 2	B3 S6	French	TP: 20	TP: 32h	TP: 64h							
Operating Systems	B3 S6	French	TP: 20			TP: 90h	TP: 60h		TP: 48h	TP: 48h	TP: 24h	
Other Institutions												
INSA Rennes, France												
Space electronics systems	M2 S8	English	CM: 14								CM: 4h	CM: 4h
UFHB, Ivory Coast												
C language and shell scripting (*,+)	L3 S5	English	CM: 57								CM: 4h	CM: 4h

Summary										
Hours	in presence	Per year	106h	210h	254h	204h	68h	192h	160h	128h	51.5h
	TD equivalents	Per year	106h	235h	305h	230h	76h	200h	168h	138h	71.5
Discharge		Per year	96h				128h		32h	64h	128h
Total hours equivalents in TD		**Per year**	**202h**	**235h**	**305h**	**230h**	**204h**	**200h**	**200h**	**206h**	**199.5h**
(1h CM = 1,5h TD)		**Total**	**2,416h**								

Remarks: During my teaching activities in tenured position I got the following teaching discharges:

- The year of my recruitment, in 2014, I benefited from a half service discharge which I used to take intensive French courses.
- The year 2020, I received a semester of Leave for Research or Thematic Conversions (CRCT) (96h) to collaborate with research center IMEC in Belgium, and a 32h discharge for the preparation of the submission of a European Research Councils (ERC) - Starting Grant, which was submitted, but not funded.
- In year 2021, I benefited from a 32h discharge for the coordination of my project financed by Agency of National Research (ANR) Young Researchers (JCJC).
- In year 2022, I benefited from a 64h discharge for the coordination of my project financed by Agency of National Research (ANR) Young Researchers (JCJC).
- In years 2023-2028 (5 years), I benefited from a 128h discharge as a Junior Member holding an Innovation Chair in the University Institut of France (IUF).

TABLE 2: Non-tenured position: Summary of teaching hours (*: Responsible)
(CM: Theory, TD: Exercises, TP: Laboratories, B: Bachelor, M: Master)

Course	Year : Semester	Language	Number students	2007-08	2009-10	2010-11	2013-14
Specification & Description Language	M1: S8	French	TP: 20				TP: 16h
Computer architecture	B2: S4	Greek	TP: 30	TP: 54h			
Basic electronic theory	B2: S3	Greek	TP: 30	TP: 122h			
VLSI Conception I	M1 : S5 & M2: S7	Greek	TD: 60		TD: 11h		
VLSI Conception II	M1 : S6 & M2: S8	Greek	TP: 30		TP: 22h	TP: 22h	
Algorithmic development & structured programming (*)	B1: S1	Greek	CM&TP: 30			CM&TP: 34h	
Electronics (*)	L2: S3	Grec	CM&TP: 30			CM&TP: 180h	
Technical industrial design & electric schematics (*)	B1: S1	Greek	CM&TP: 30			CM&TP: 60h	
Introduction to computer science (*)	B1: S1	Greek	CM&TP: 30			CM&TP: 30h	
Accounting and Spreadsheets (*)	B2: S3	Greek	CM&TP: 30			CM&TP: 42h	
Total hours			**Per year**	**182h**	**33h**	**368h**	**16h**
			Total	**599h**			

The following list briefly outlines the courses taught and the total hours per course:

- **INSA (France) - Associate professor (2022-present):**
  - *Space Electronic Systems (CM: 8h (12h eq. TD)):* Course taught in 10^{th} semester, i.e., second year of master (M2), in English in national master "Electronics and Telecommunications". This course presents the sources of fault in electronic systems, several ways to analyze the system vulnerability and faul-tolerant approaches to enhane system reliability in hardware and software.
- **UFHB (Ivory Coast) - Associate professor (2022-present):**
  - *C language and shell scripting (CM: 8h (12 eq. TD):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in computer science in English. The first part of the course is dedicated to the use of the Linux operating system and scripting languages. In the second part, students discover the functioning and use of the C language.
- **ISTIC (France) - Associate professor (2014-present):**
  - *Multitasking Operating Systems (CM: 60h (120h eq. TD)):* Course taught in 7^{th} semester, i.e., first year of master (M1), in English in international master "EIT Digital Cloud Computing and Services" and in national master "Software Engineering". This course presents resource and time allocation, problems and solutions for cooperation and competition between processes, implementation and use of virtual memory and paging.
  - *C language and shell scripting (CM: 96.5h (168.75h eq. TD), TD: 48h (60h eq. TD), TP: 180h):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in computer science in English. The first part of the course is dedicated to the use of the Linux operating system and scripting languages. In the second part, students discover the functioning and use of the C language.
  - *Computer programming (CM: 15h (22.5h eq. TD):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in the professional licence of electrical and embedded systems in French. The students discover the compilation and debugging tools, the functioning and use of the C language.
  - *Introduction to Linux (CM: 4.5h (6.75h eq. TD):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in the Computer Methods Applied to Business Management bachelor. The students discover the use of the Linux operating system and scripting languages.
  - *Hardware accelerators for AI (TP: 7.5h):* Course taught in the 9^{th} semester, i.e., second year of master (M2), in the Embedded System master. The students study the use of specific hardware to execute AI models.
  - *Computer architecture 1 (TD: 54h, TP: 96h):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in computer science. The objective of is to teach the students the methods of realization

of combinatorial circuits, the design of sequential circuits and the realization of control units.
  - *Computer architecture 2 (TD: 32h, TP: 72h):* Course taught in the 6^{th} semester, i.e., third year of bachelor (B3), in computer science. The students learn the principles of operation of a programmable processor, the assemble language, memory management, inputs/outputs, etc.
  - *Principles of computer operation (TD: 40h, TP: 120h):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in computer science. Students learn the basic skills in designing digital circuits and programmable processor over FPGA platforms.
  - *Software/hardware interface (TD: 36h, TP: 96h):* Course taught in the 6^{th} semester, i.e., third year of bachelor (B3), in computer science. The students learn how programs are complied to assembly and machine language, how memory management takes place and how I/O operations are implemented from/to peripheral devices.
  - *Operating Systems 1 (TP: 72h):* Course taught in the 5^{th} semester, i.e., third year of bachelor (B3), in computer science. The objective of this module is to use the basic commands associated with the Linux operating system and Linux file management.
  - *Operating Systems 2 (TP: 160h)* and *Operating Systems (TP: 246h):* Course taught in the 6^{th} semester, i.e., third year of bachelor (B3), in computer science. Students learn about system calls, processes and their communication through shared memory, semaphores, layers and the basics of network protocols. The students implement implement an audio streaming system between a server and multiple clients.
- **ENSEEIHT (France) - Teaching assistant (2013-2014):**
  - *Specification and Description Language (SDL) (TP: 16h):* Course taught in the 8^{th} semester (M1). We teach students the principles of programming in SDL. They have a short project, which consists in developing an alternating bit protocol.
- **TEI (Greece) - Non-tenured lecturer (2010-2011):**
  - *Algorithm development & structured programming (CM & TP: 34h):* Department of Business and Information Systems Planning, which is a 1^{st} semester course (B1). Students learn the principles of programming and the C language.
  - *Electronics (CM & TP: 180h):* Mechanical Department, which is a core course in the 3^{rd} semester (B2). Students learn to build electronic circuits with resistors, cables, generators capacitors, inductances and learn to use multimeters, voltmeters, ammeters and oscilloscopes to measure oscilloscopes to measure various metrics, to observe and analyze circuit behavior.
  - *Technical Industrial Design and Electrical Schematics (CM & TP: 60h):* Department of Electrical Engineering, which is a basic course of the 1^{st} semester (B1). Students learn how to draw electrical and mechanical schematics. They also learn the principles of developing an electrical installation. They have a project that consists of developing an electrical installation for a three-story building.
  - *Introduction to Computer Science (CM & TP: 30h):* Speech and Language Department, which is a core course of the 1^{st} semester (B1). Students learn the structure of a computer and how to use programs.
- **VINT (Greece) - Non-tenured lecturer (2010-2011):**
  - *Accounting and spreadsheet (CM & TP: 42h):* Department of Administration and Financial Management, which is a 3^{rd} semester (B2) course. Students learn spreadsheet manipulation and advanced features.
- **ECE (Greece) - Non-tenured lecturer and teaching assistant (2009-2011):**
  - *VLSI Design I, (TD: 11h):* An electronics and computer science course, taught in the 7^{th} and 9^{th} semesters (M1 & M2). The main topic is semiconductor technology, design rules, resistance estimation design, resistance and capacitance estimation, transistor size and logic structures CMOS.
  - *VLSI Design II (TP: 44h):* An electronics and computer science course taught in 8^{th} and 10^{th} semesters (M1 & M2). The main topics are clocking strategies, logic and memory structures and memory structures, CMOS design methods, RTL synthesis, logic optimization. The students learn PSpice and VHDL and design several systems with adders, subtractors ALU, multipliers, memory elements. Finally, they have a project in VHDL and PSpice at the end of the course.

- **CEID (Greece) - Teaching assistant (2007-2009):**
  - *Computer architecture (TP: 54h):* Course taught in the 4^{th} semester (B2). We teach students the principles of assembler programming. The programming is done on the AT91SAM9261EK platform (ATMEL) and the KEIL simulator.
  - *Basic electronics (TP: 126h):* Course taught in the 3^{rd} semester. The students learn to build electronic circuits with resistors, cables, generators, capacitors, inductance, transistors and learn to use multimeters, voltmeters, ammeters and oscilloscopes to measure to measure several metrics, observe and analyze the behavior of the circuit.

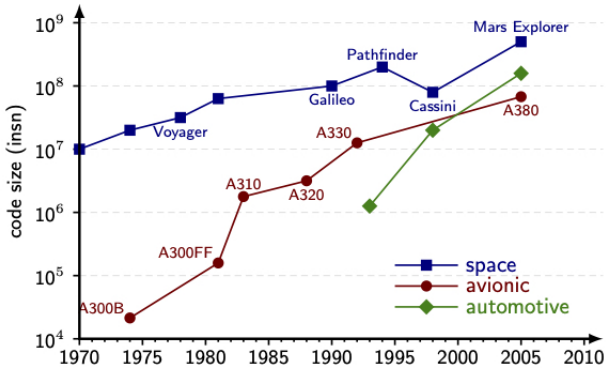
5 Research activities

Keywords : Dependability, Reliability, Safety, Energy Efficiency, Embedded systems, Computer Architecture, Design Space Exploration, Optimisation, Run-time Adaptation, Protection and Control Mechanisms.

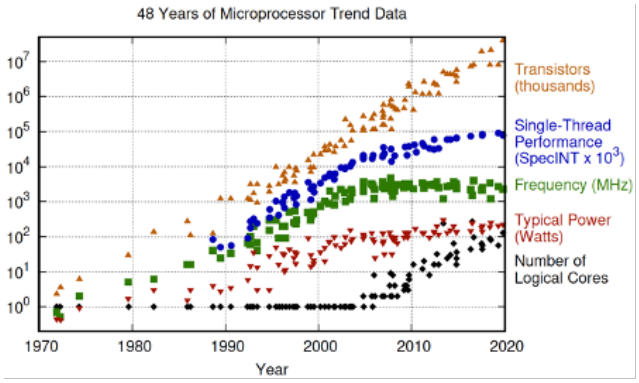
5.1 Context and overall goal

Critical industries are specialized in domains that rely 95% on embedded systems [8]: fly-by-wire systems are used in avionics [18] (Airbus, Thales, ONERA, etc.), navigation systems in space [18] (ESA, DLR, CNES, etc.), automatic braking systems in automotive [16] (Peugeot, Volkswagen, Scoda, etc.), insulin pumps in the health-care [15] (Siemens Healthineers, Philips Healthcare, etc.), embedded vision systems in surveillance [25] (Ivisys, Datalogic, IRIDA-Labs etc). In these domains, applications are becoming more and more complex and their computational demands scale rapidly. As shown in Figure 1a, the code size of automotive, space and avionics applications has significantly increased within thirty years, e.g., more than three orders of magnitude in avionics [5], while future automotive and avionic applications will require higher computing resources [4]. To address these demands, architectures with multiple processing elements (cores), able to concurrently execute a high volume of applications [12], and application specific hardware accelerators, tailored to the needs of the application [10], are required. This evolution of the hardware complexity is witnessed in Figure 1b.

Dependability is a requirement for embedded systems deployed in such critical domains, as they must deliver services that can be trusted within a time-period, even when the system is subject to natural failures or malicious attacks. Main aspects of dependability include *reliability*, *safety* and *security*, which are essential attributes of trustworthy systems. Dependable systems should be designed to deliver services as specified, to operate without catastrophic failure and to be protected against attacks.



(a) Code increase in safety-critical industry [5].



(b) Evolution of platform complexity [22].

Reliability is under threat due to the increased fault susceptibility of modern electronic systems. Reliability threats, such as manufacturing process variation, aging, temperature and radiation, introduce hardware faults to the system by corrupting the stored information, the computations and the communications. Such faults can change the expected output of the application, compromising the system's correct operation,

potentially leading to catastrophic consequences for the system and the user. Typical reliability solutions, that rely on full hardware or software redundancy, usually entail significant cost, latency and resource overheads, which are often not suitable for critical embedded systems, which are resource constrained. To cost-effectively address these reliability threats, the system must be properly analysed in order to identify the most vulnerable software and hardware parts [19], and enhanced with effective protection mechanisms [6].

Safety is highly linked hard real-time guarantees in critical domains. Not only the application's result should be correct, but also it should be generated in-time, within the deadline. To provide timing safety, the worst case of the system execution has to be considered during system analysis and design [14]. However, the real Worst-Case Execution Time (WCET) of an application is generally unknown, and thus, a safe estimation of the WCET must be obtained. Application and hardware platform complexity [9], e.g., multiple execution paths, dynamic hardware components and shared hardware resources, introduces unpredictability to the system's timing behavior, which has to be upper bounded in order to be safe. This naturally overestimates the real WCET [17], leading to pessimistic WCET estimations, up to $\times 7$ more [C8, 24], and thus, under-utilisation of system resources. To reduce the WCET pessimism, and thus, improve system efficiency, run-time approaches are a promising solution, as they take advantage of the information that becomes available only during execution.

Security is in danger due to malicious attacks, such as fault injection and side-channel analysis, that have as a goal to recover secret assets, alter the expected performance and render the system useless through denied access or reduced quality or performance. Security countermeasures, such as complex cryptography algorithms and redundancy, help to detect and mitigate these threats. However, such typical solutions have high overhead, being a concern for critical embedded systems, because of their constraints in power consumption, area, cost, and timing. Therefore, efficient means are required to perform analysis of the system vulnerability and to design security countermeasures, that have low overhead, and thus, are appropriate for critical embedded systems.

Meanwhile, the *sustainability* of electronic systems has become of paramount importance. The amount of electronic devices is increasing day by day. Combined with the increased complexity of applications, such as Artificial Intelligence (AI), and the computation capabilities of modern hardware platforms, the amount of consumed electricity of electronic devices is significantly increased, negatively impacting the environment. To reduce this negative impact, energy efficient electronic devices should be designed, the lifetime of the electronic devices should be extended and e-waste should be minimized [2]. Several approaches have been established to maximize system energy efficiency, such as Dynamic Voltage and Frequency Scaling (DVFS) [26] and approximation in computation and communication [1] in domains that can tolerate imprecise results, such as image processing, data mining, machine learning, etc. However, such approaches usually have a negative impact on reliability, safety and security, e.g., reducing supply voltage/frequency increases the execution time and the transient fault rate [27].

To provide dependable critical embedded systems, enhancing digital sustainability, efficient analysis and deployment approaches, along with run-time adaptation capabilities, are required. However, designing such systems is perplexing and tedious process, as it consists of several interdependent NP-hard problems [B2] in a large multi-dimensional design space [11], with constraints and trade-offs among reliability, execution time, security, aging and energy efficiency. In this context, applying exhaustive Design Space Exploration (DSE) is infeasible. Trial-and-error approaches, based on the designers' experience, usually require several design iterations, being time-consuming without any upfront guarantee that the system will satisfy the application constraints [J6]. DSE methodologies are required with reduced exploration time leading to near-optimal solutions. Furthermore, as design-time approaches cannot take advantage of the information created during the system execution, they have to be combined with run-time approaches in order to provide further improvements.

5.2 Summary of main contributions

In this context, I have worked on several novel analysis and DSE approaches, along with protection and control mechanisms, to deal with reliability and timing safety, applied at design-time and at run-time at different abstraction layers of critical embedded systems, as described below.

5.2.1 Reliability

The reliability aspect is addressed by approaches that a) analyse the system vulnerability and b) propose protection mechanisms. I worked on approaches that address reliability regarding the overall system deployment and execution (focusing on RISC-V, FPGA and GPU platforms), the computations of processing elements and the communication over Network-On-Chips (NoC), with a high interest on Neural Networks (NNs), which insert additional challenges due to their large model size and architecture. We have published a survey and a framework that systematically classifies reliability protection mechanisms in [J21].

a) Vulnerability analysis is performed by injecting faults into the system and observing its behavior. Fault injection can be done by hitting the real system with irradiation and by simulating the impact of injected faults. The first method provides realistic results, but it is a black box approach lacking fault propagation visibility. The second method allows a more detailed analysis, but the results are less realistic and the analysis may take long time, depending on the fault model and the abstraction layer. To obtain realistic and effective vulnerability analysis, hybrid approaches are required across abstraction layers.

Towards this direction, we proposed a cross-layer analysis based on fault injection through simulation, from the semiconductor layer up to the application layer [C29, C20]. We focused on transient faults caused by single radiation particles and used as a case-study a RISC-V processor. At a first step, we analysed particles with different characteristics hitting cells of the technology under study to obtain the fault models, including transient pulses of different widths. As a second step, these fault models are injected at the gate-level description of the design through a single-cycle simulation. The observed errors are used as models to a higher abstraction layer, where they are injected to a Cycle-Accurate Bit-Accurate (CABA) microarchitecture-level simulator running the applications. Combining the analysis across layers, the vulnerability results remain accurate, whereas the analysis time is significantly reduced compared to low-level fault injection. Our second cross-layer analysis combines neutron beam experiments and fault injection through simulation. Our case study is General Matrix Multiplication (GEMM), Neural Networks (NNs) [J26] and Vision Transformers (ViTs) [C48, C32] on GPUs. As a first step, we perform neutron beam experiments with the kernels in order to obtain realistic fault models and error rates. As a second step, we conduct software fault injection, tuned with the experimentally observed fault models under beam. Following this approach, we have shown that real fault models are more complex than commonly used single bit-flips, and we can track the propagation of faults and identify the faults that are more likely to corrupt inferences.

Vulnerability analysis through beam experiments under high-energy neutrons has been performed for RISC-V and FPGA platforms. We analysed the functional and timing behavior of several benchmarks, including a quantized Convolutional Neural Network (CNN), running sequentially and in parallel on a RISC-V ASIC multicore platform [C26, PP14, PP9, PP4]. We observed that the errors are directly related on how the application uses the platform resources. Synchronisation and memory intensive applications have higher Detectable Unrecoverable Error (DUE) rate, while compute-intensive applications have higher Silent Data Corruption (SDC) rate. We have also analysed the impact of the parameters of High-Level Synthesis (HLS) tools, used to design hardware accelerators, on the vulnerability of the NN hardware accelerators [J33, PP11, PP13]. We observed that tweaking hardware parameters, such as the reuse of resources, can increase the error rate linearly.

Furthermore, we proposed a hybrid framework to assess the vulnerability of NNs [C37, C34] in order to identify the critical parameters and bits. As a first step, we perform datatype-and-layer-based fault injection at the software level, driven by the NN characteristics. As a second step, we use classification-based machine learning methods in order to predict the criticality, not only of network parameters, but also of their bits.

Last, we performed an accurate vulnerability analysis for NNs through software fault injection, where we study the fault impact, not only on the weights, but also on biases and intermediate data, considering the criticality of layers, the data-types and the direction of bit change due to faults [C47, C33]. We observe that, except for the last layer, faults transitioning from 0 to 1 significantly impact the classification outcome.

b) Protection mechanisms have been proposed both at the hardware layer and at the application layer to deal with hardware faults on the function units of processors, the NoC and the memory.

i) Hardware layer. We have proposed hardware mechanisms to protect faults in the function units of heterogeneous Very Large Instruction Word (VLIW) processors. The main idea is to explore the idle slots in the current and next instruction bundles (i.e., a set of instructions executed concurrently by VLIW processors) and prioritize dependent instructions. The mechanism performs instruction triplication considering short-term transient faults [C11, J25]. We leveraged this mechanism for permanent faults, where instruction triplication and re-scheduling is applied taking into account the status of the function units [C10]. To reduce the performance degradation due to the instruction replication, dynamic instruction re-scheduling is applied based on the status of faulty FUs in a coarse-grained [C15] and a fine-grained way [C17].

Hardware mechanisms have been proposed for mitigation of permanent faults impacting the packets transferred through a NoC datapath [C23, C22]. The main idea is to re-organize the flits at the subflit scale in the router, moving the fault impact on the Least Significant Bits (LSB). Critical data, such as headers, are handled by redundancy, where the critical information is distributed on two flits. The proposed approach deals with high fault densities contrary to state-of-the-art methods, such as the extended Hamming code, with small critical path and latency overheads. To further reduce hardware overheads, a region-based version [J23] is proposed, which protects regions, instead of routers. Reliability efficiency and hardware costs can be traded-off through different subflit and region sizes, leading to reduced hardware costs with small impact on the reliability efficiency.

Last, to protect faults occurring in NN parameters with reduced overhead, we proposed a set of selective hardware mechanisms. Our first approach detects and mitigates the fault impact on NN by forcing the faulty values to zero instead of correcting them [C47, C33]. This light-weight solution duplicates sensitive flip-flops and inserting AND gates to drive the hardware design. The obtained results show that the proposed approach has low area and critical path overhead, compared to existing approaches, while keeping the accuracy high. Our second approach proposes a set of dedicated Error Correction Codes (ECCs) in the memory, which are selectively inserted to protect only the critical parameters and bits of NNs [C37, C34]. The results show that it is possible to protect the critical network parameters, while saving up to 83% memory compared to conventional ECC approaches.

ii) Application layer. We proposed low-cost mitigation approach that reduces the impact of transient faults on ViTs on GPUs [C48, C32]. The idea is to modify the Identity layers within the ViT Block in order to prevent the propagation of corrupted values that can generate critical SDCs, such as inf, NaN, and large values. The observed results show that the proposed approach can correct 90.7% of critical failures, with execution time overheads as low as 5.61%.

5.2.2 Timing safety

The safety aspect has been addressed through approaches that provide timing guarantees for critical embedded systems. The proposed approaches focus on design-time DSE for timely safe system deployment and run-time control mechanisms to safely adapt the system execution.

a) Design Space Exploration. In several hard real-time application domains, less accurate results, computed before the deadline, are preferable than accurate, but too late, results [3]. This is due to the fact that a real-time application has to provide a result before its deadline in order to be considered as safe. When not enough time is available, approximate results are acceptable, as long as the minimum acceptable Quality-of-Service (QoS) is satisfied and the results are provided in time [7]. For such Imprecise Computation (IC) applications, a set of decomposition-based deployment approaches has been proposed to

guarantee timely safe and energy efficient system execution. An algorithm is designed to provide the optimal solution for independent IC tasks executed on a symmetric multiprocessor [C12], which has been extended for platforms with DVFS capabilities [J15]. We have leveraged our decomposition-based solution for dependent IC tasks and heterogeneous multicore platforms and proposed an accelerated, but still optimal, version of our decomposition-based method [J16]. Last, optimal and heuristic approaches considering task migration are proposed in order to take advantage of asymmetric multiprocessors, such as big.LITTLE platform [C16].
b) Run-time control mechanisms. To reduce the WCET pessimism, information from the task scheduling and allocation can be used to compute interference-sensitive Worst-Case Execution Time (isWCET) [21, 23, C13, 20], which accounts for the interference only of the tasks scheduled in parallel. However, such isWCET are schedule and allocation dependent, and thus, they are valid only for the solution they have been estimated for. In order to guarantee a timely safe execution, the solution, used to compute the isWCET, has to be maintained during execution. Otherwise, additional interferences may occur, which have not been accounted for during task scheduling and allocation, jeopardising safety. To achieve that, time-triggered execution is usually used, which, however, does not allow any performance improvement. Therefore, we proposed a run-time mechanism that inserts control phases on each core with a fine-grained protection that allows the tasks to be executed earlier than time-triggered execution, whenever is safe [C18]. Our second contribution [C21] comes from the observation that by enforcing the partial order of tasks, we limit the performance improvement that can be achieved through run-time adaptation. To further improve performance gains, we leverage our approach with a safe relaxation of the partial order of tasks. The obtained results on an eight-core TI platform show that the fine-grain synchronisation and the dynamic adaptation provide performance improvements, guaranteeing safety.

Furthermore, existing approaches are based on WCET estimations obtained during design-time, and thus, they are not able to take advantage of the information available during execution. To deal with this limitation, we proposed a run-time control mechanism that computes new safe estimations of the WCET during execution, based on the task progress. The updated WCET estimations are used to derive the available time-slack and postpone mode switch in mixed-critical systems [C8, C7, C9, W1]. The mechanism is leveraged to dynamically decide when to invoke the controller, reducing the controller's overhead, further increasing the gains [J14]. Last, we extend this mechanism in order to support preemptive execution of tasks [J28]. The evaluation results on the eight-core TI platform show that the proposed mechanisms have lower cost and achieve significant improvements in avoiding mode-switch, compared to existing approaches, while guaranteeing safety.

5.2.3 Reliability and Timing Safety

The majority of approaches consider independently reliability and timing safety. However, hardware faults can degrade the hardware components, due to permanent faults, or modify the execution flow, due to temporary faults, potentially increasing the execution time, and thus, impacting timing safety. Few approaches address the impact of hardware faults to the timing behaviour of applications, but they target only memories. Nonetheless, with technology size reduction, faults in combinational logic and sequential logic of processors cannot be considered negligible anymore [13].
a) Vulnerability analysis is enhanced to include not only functional correctness, but also timing correctness. On top, we combine it with a Measurement-Based Probabilistic Timing Analysis (MBPTA) WCET estimation in order to be able to fault-aware WCET estimations, under faults in processors [PP10, C36, C35, PP15, C27]. As a first step, a statistical fault injection through bit-flips is performed on the pipeline registers of the processor (a RISC-V is used as a case-study). We collect not only the vulnerability metrics regarding functional behavior (Crash, Hang, Application Output Mismatch and Internal State Mismatch), but also execution cycles describing timing behavior (Execution Cycle Mismatch). As a second step, the Extreme Value Theory (EVT) and Block Maxima (BM) are applied on the measured traces to obtain probabilistic WCET estimations under hardware faults in the processor. The obtained results show that such faults can

significantly impact the timing behaviour, and thus, the WCET estimations and safety.

b) Protection mechanisms have been proposed at the hardware layer with safe upper bounds and at the deployment layer, taking into account the WCET overhead due replication, providing reliable and timely safe deployment.

i) Hardware layer. We design intrusive, fine-grained lockstep processors with a safe and low upper bound time for error detection and correction using HLS [C38, C35, C36, C35, PP15]. Two processors are running the same task with the same set of inputs and shadow registers are used to keep the last correctly executed instruction. A consistency check is applied between the pipeline registers of both cores at each cycle. Whenever an error is detected, recovery is performed by copying the content of the shadow registers to the pipeline registers. The timing overhead is upper bounded to two clock cycles. To reduce the area overhead of the shadow registers, the second approach stores only the address of the instruction and re-fetch is applied in case of an error. The upper bound of the timing overhead equals to the depth of the processor pipeline, which is five in our RISC-V use case.

ii) Deployment layer. Efficient DSE is required in order to achieve reliable and safe task deployment with low energy consumption. We proposed DSE approaches to deploy parallel applications on homogeneous multicore platforms with DVFS, with the goal of minimizing total energy consumption, under real-time and reliability constraints. The approaches decide task allocation, task scheduling, frequency assignment, and selective task duplication considering three possible DVFS schemes, i.e., task-level, processor-level and system-level, for independent tasks [C19, J29] and dependent tasks [J24, C24]. Both optimal and heuristic algorithms have been proposed for each DVFS scheme. Experimental results show that the proposed approaches achieve better energy saving and ability to obtain feasible solutions. To take into account the inter-processor communication, a task deployment DSE has been proposed for NoC-based multicore platforms with DVFS [C28, J34], that balances the overall energy consumption, under reliability and real-time constraints. The deployment process jointly optimizes frequency assignment, task allocation, task scheduling, task duplication and path selection. Moreover, a novel heuristic method is proposed to enhance scalability, achieving good solutions with low computation time.

5.2.4 Security

Reliability is related to the protection of the system from unintended faults, whereas security focuses on protecting systems from intentional threats, such as malicious attacks. Although the way of physically impacting the system is different, e.g., radiation particles vs ElectroMagnetic (EM) interference, the physical impact to the system hardware is similar, leading to similar fault models, e.g, bit-flips and transient pulses altering the information stored, impacting the computations and the communications. While they may seem distinct, fault tolerance and security are closely intertwined, sharing a significant common ground, revolving around vulnerability analysis and protection methods.

We have recently started to explore vulnerability analysis for security. During an internship in 2023, we perform EM experiments for a mutlicore RISC-V platform and software fault injection. An internship just started will explore the EM attacks on ViTs on GPU and another will start on analysing the attacks on cache multi-socket systems through flush instructions. Furthermore, I am participating in the discussions with IETR in order to be able to use their laser equipment to perform laser fault injection in RISC-V, FPGA and GPU platforms, and in the CYBERPROS project, having as goal the vulnerability analysis and protection methods of RISC-V processors. Our cross-layer vulnerability analysis based on fault injection through simulation can be used to inject security fault models at micro-architecture level, such as instruction skip, and at low-level by jeopardizing the processor control signals, including the clock and the write enable signals.

5.2.5 Other works

During my carrier, I have also contributed in designing embedded systems for performance and energy consumption improvements, through methodologies for architecture design, mapping data in the memory hierarchy and system deployment. More precisely, I have worked on the DSE for embedded Application Specific Instruction-set Processors (ASIP) for on-line biotechnology monitoring applications having as design objectives the low-cost and the low-energy consumption [C2]. The result of our DSE methodology has lead to an ASIP architecture that has been patented [P1] and the steps of the proposed DSE methodology have been published as scientific book edited by Springer [B1]. I focused on data mapping methodologies [J1, J2, J5, J4, J3, J9, J8, J10, J11, J13, J12, PP2], DSE methodologies for domain-specific SoftWare/HardWare (SW/HW) architectures [J6, BC1, C1, C5] and scheduling and assignment techniques [J7] having as main objective to improve the system performance. A part of my work was on run-time control of packets in Wireless Sensor Networks (WSNs) having as goal the reduction of the transmission latency, the packet loss and the energy consumption [C4, C6, C3]. Optimal and heuristic DSE approaches have also been proposed to schedule, allocate, adjust and configure the task execution and packet transmission on WSNs [BC2, J17, J20, C14, J19, J18, J22, J30], under energy and real-time constraints, having as objective the global energy improvements. Last, an extended version of the thesis has been published as scientific book edited by Springer [B2].

5.3 Publications

Table 4 summarises the number and the quality of publications classified by patent, scientific book, scientific book chapters, international journals with review process along with the corresponding Scientific Journal Ranking (SJR: Q1, Q2, Q3, Q4), papers published in international conference with review process and procceding along with the corresponding Qualis ranking (A1, A2, B1, B2, B3, B4). It also summarizes other publications in international publications without proceeding and national conferences. Section 5.8 provides the complete publication list.

TABLE 4: Summary of publications.

International publications with proceedings

(†Special Sessions, $^{+}$Extended Abstract, *WiP, ‡ Educational Classes)

Type		**2010**	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**	**Total**
Patent (EP-US)		**1**															**1**
Scientific books (Springer)		**1**				**1**											**2**
Scientific book chapters		**1**								**1**							**2**
Int. journals		**-**	**1**	**1**	**5**	**2**	**2**	**2**	**-**	**4**	**3**	**1**	**2**	**4**	**4**	**4**	**35**
SJR	Q1		1		1					2	2	1	2	1	3	2	15
	Q2				1	2	1	1		1	1			1	1	2	11
	Q3			1	3			1		1				2			8
	Q4						1										1
	–																-
Int. conferences		**2**	**1**	**3**	**1**	**2**	**-**	**1**	**4**	**1**	**4**	**5**	**2**	**5**	**9**	**9**	**51**
Qualis	A1				1*				1†		3			1,1†	1+,1†	2	11
	A2					1			1			2,1*	1		1	1†, 1‡	9
	B1		1	1					1	1		1	1	1,1†	1†	2, 1†	12
	B2			1								1			1	1†	4
	B3			1											3	1,1†	6
	B4	2							1					1			4
	–					1		1			1				1	1	5
Total		**5**	**2**	**4**	**6**	**5**	**2**	**3**	**4**	**6**	**7**	**6**	**4**	**9**	**13**	**8**	**90**

Other international and national publications

Type	**≤2010**	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**	**Total**
Inter.Conf. w/o proceedings	-	-	-	-	**1**	**1**	-	-	**1**	-	-	-	**5**	**7**	**1**	**16**
Poster	-	-	-	-	1	-	-	-	-	-	-	-	1	3	-	5
Oral Presentation	-	-	-	-	-	1	-	-	1	-	-	-	4	4	1	10
National conferences	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**3**	**1**	**7**
Thesis	**2**	**-**	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**-**	-	**4**
Rapports techniques	**1**	**2**	**-**	**-**	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**1**	**-**	**-**	-	**5**

5.4 Supervision

Table 5 summarises the number of post-docs, Ph.D. students and Master and Bachelor students I have (co-)supervised.

TABLE 5: Summary of supervised students (C: Current, D: Defended, A: Abandon)

Type	**Post-doc**	**PhD**	**Master Internships**	**Bachelor Internships**
Number	5	3xC, 4xD, 1xA	8	9
Total: 30				

Postdoctorant

05/2024 - 04/2026	**Raphael Billig Tonetto**
Title	"Analysis and Design of Domain-Specific Reliable Processors"
Funds	ANR JCJC FASY
01/2022 - 12/2023	**Fernando Fernandes dos Santos**
Title	"Toward reliable deep neural network hardware for safety-critical applications"
Funds	MSCA Bienvenue Fellowship
Publications	[PP9, J26, C26, PP8, PP6, PP4, C32, PP14, PP12]
10/2021 - 09/2022	**Marcello Traiola**
Title	"Emerging paradigms for resilient computing"
Funds	INRIA fellowship
02/2021 - 12/2022	**Arash Nejat**
Title	"Fault-tolerant RISC-V processor"
Funds	FLODAM project and Stratégie d'Attractivité Durable (SAD) fellowship
04/2017 - 04/2019	**Lei Mo**
Title	"Task mapping optimization methodologies for multicore architectures"
Funds	Stratégie d'Attractivité Durable (SAD) fellowship
Publications	[BC2, J15, J16, J17, J19, J18, J20, J22, C12, C14, C16, PP3]

Doctorants

Current

09/2024 -	**Lucas Roquet**
Title	"Dependability Evaluation and Enhancing Methods for Large Machine Learning Models"
Direction	100%
Supervision	30% with Fernando Fernandes dos Santos (70%)
Funds	Ministère de l'Enseignement Supérieur et de la Recherche (MESR) fellowship
09/2022 - now	**Romaric Nikiema**
Title	"Time-guaranteed and reliable execution for real-time multicore architectures"
Direction	100% [1]
Supervision	50% with Marcello Traiola (50%)
Funds	Contract ANR JCJC (FASY)
Publications	[C38, C36, C35, PP10, PP15, N4]
09/2022 - now	**Wilfread Guilleme**
Title	"Fault-tolerant architectures for artificial intelligence algorithms"

[1] Derogation HdR obtained

Supervision	33,3% with Daniel Chillet (33,3%) and Cedric Killian (33,3%)
Funds	Direction Générale de l'Armement (DGA) fellowship and INRIA fellowship
Publications	[C47, C33, N6, N5]

Former

11/2021 - 01/2025	**Seungah Lee**
Title	"Efficient designs of on-board heterogeneous embedded systems for space applications"
Supervision	35% with Emmanuel Casseau (30%) and Ruben Salvador (35%)
Funds	Centre National des Etudes Spatiales (CNES) fellowship and Contrat Doctoral Ordinaire - Université Rennes 1 (CDO) fellowship
Publications	[C30, C39]
09/2018 - 06/2022	**Minyu Cui**
Title	"Energy-Quality-Time fault tolerant task mapping on multicore architectures"
Supervision	60% with Emmanuel Casseau (40%)
Funds	École Normale Supérieure (ENS)/China Scolarship Council (CSC) fellowship
Publications	[C19, C24, J24, J29, PP7]
10/2018 - 12/2021	**Romain Mercier**
Title	"Multiple Fault Mitigation in Network-on-Chip Architectures Through a Bit-Shuffling Method"
Supervision	35% with Daniel Chillet (30%) and Cedric Killian (35%)
Funds	Direction Générale de l'Armement (DGA) fellowship and INRIA fellowship
Publications	[C22, C23, J23, PP5, N3, N1, N2]
09/2018 - 09/2020	**Joseph Paturel ***
Title	"Design-space exploration of fault tolerant multicores"
Supervision	50% avec Olivier Sentieys (50%)
Funds	Contract RAPID/DGA (FLODAM)
Publications	[C20]
	* Stopped PhD at the beginning of 3rd year
09/2015 -12/2018	**Rafail Psiakis**
Title	"Self-healing mechanisms for vector processors"
Supervision	70% avec Olivier Sentieys (30%)
Funds	Ministère de l'Enseignement Supérieur et de la Recherche (MESR) fellowship
Publications	[C10, C11, C15, C17, J21]

International internships

09/2020 - 06/2023	**Xinmei Li** (3-year Master thesis) M1-M2-M3 Computer Science School of Automation Southest University, China
Title	"QoS-aware Imprecise-Computation task mapping on heterogeneous multicores"
Supervision	with Lei Mo
Publications	[TR4, J27]
09/2019 - 06/2022	**Qi Zhou** (3-year Master thesis) M1-M2-M3 Computer Science School of Automation Southeast University, China

Title	"Energy-aware Imprecise-task mapping for Wireless Network Systems"
Supervision	with Lei Mo
Publications	[C28]

National internships

09/2024 - 12/2024	**El Mehdi Belhaddad** M1 INP Bordeaux France
Title	"Reliability Assessment of Processing-In-Memory (PIM) Architectures"
	with F. dos Santos, M. Traiola
06/2024 - 07/2024	**Augustin Lucas** L3 ENS Lyon France
Title	"Characterization of the clflush Instruction on Multi-Socket Systems"
Supervision	with Guillaume Didier
05/2024 - 08/2024	**Erwan Le Carrer** L3 Computer Science UFR ISTIC University of Rennes, Rennes, France
Title	"Fault Tolerance Assessment and Improvement of Approximate Hardware Accelerators for Artificial Intelligence"
Supervision	with Marcello Traiola
05/2024 - 08/2024	**Leah Laurant** L3 Computer Science UFR ISTIC University of Rennes, Rennes, France
Title	"Simulating Realistic Radiation-induced Fault Effects on GPUs at the Software Level"
Supervision	with Fernando Fernades dos Santos
05/2024 - 08/2024	**Raphael Denis** L3 Computer Science UFR ISTIC University of Rennes, Rennes, France
Title	"Vulnerability analysis of RISC-V processors"
Supervision	with Fernando Fernades dos Santos and Marcello Traiola
03/2024 - 08/2024	**Lucas Roquet** M2 Cyber-Security UFR ISTIC University of Rennes, Rennes, France
Title	"Improving Security and Reliability of Large Vision Transformers Models on Embedded GPUs"
Supervision	with Fernando Fernades dos Santos and Marcello Traiola
Publications	[C48]
05/2023 - 08/2023	**Lucas Roquet** M1 Cyber-Security

	UFR ISTIC
	University of Rennes, Rennes, France
Title	"Characterizing the impact of radiation-induced errors on Vision Transformers for NVIDIA GPUs"
Supervision	with Fernando Fernades dos Santos and Marcello Traiola
Publications	[C48]
05/2023 - 08/2023	**Thomas Feuilletin**
	L3 Computer Science
	UFR ISTIC
	University of Rennes 1, Rennes, France
Title	"Analytical methods for vulnerability analysis of hardware circuits"
Supervision	with Joseph Paturel and Marcello Traiola
05/2023 - 08/2023	**Melanie Romano**
	L3 Computer Science
	UFR ISTIC
	University of Rennes 1, Rennes, France
Title	"Electromagnetic attacks on RISC-V multicore architectures"
Supervision	with Fernando Fernades dos Santos and Marcello Traiola
06/2021 - 08/2021	**Nitesh Narayana**
	M2 Computer Engineering
	Indian Institute of Information Technology Design and Manufacturing
	Kancheepuram, Indie
Title	"Hardware acceleration of LSTM neural network based on High-Level Synthesis"
Supervision	with Olivier Sentieys
03/2021 - 08/2021	**Mouad Moatassim Billah**
	M1 Embedded systems and microsystems
	Faculty of Science and Engineering
	University of Paul Sabatier, Toulouse, France
Title	"Run-time management of mixed-critical systems on multicore platforms"
03/2021 - 06/2021	**Abdelrahman Ahmed Azab**
	M2 Engineering of complex systems
	National Institute of Applied Sciences (INSA), Rennes, France
Title	"Efficient designs of on-board heterogeneous embedded systems for space applications"
Supervision	with Olivier Sentieys
05/2021 - 07/2021	**Remi Robilliard**
	L3 Computer Science
	UFR ISTIC
	University of Rennes 1, Rennes, France
Title	"Remaining Worst-Case Execution Time computation with performance counters"
05/2018 - 07/2018	**Thomas Razafindralambo**
	L3 Computer Science
	UFR ISTIC
	University of Rennes 1, Rennes, France
Title	"Processor vulnerability analysis and error modeling"
05/2015 - 07/2015	**Thibaut Marty**
	L3 Computer Science

	UFR ISTIC
	University of Rennes 1, Rennes, France
Title	"Dynamic run-time control for mixed-critical systems running on multi-core COTS"
Publications	[J14, C9]

5.5 Projects and contracts

Table 6 summarises the International and National research projects and other national research contracts, in which I have participated.

TABLE 6: Summary of projects and contracts (PI: Principal Investigator, WPL: WorkPackage Leader).

	Projects		**Contracts**
Type	**International**	**National**	**National**
Number	6	7	5
	1 x EDF (WPL) 2 x FP7 1 x H2020 1 x ENIAC/ARTEMIS 1 x Leonardo da Vinci	1 x ANR JCJC (PI) 1 x ANR PRCE 1 x DGA/RAPID 1 x Regional 1 x ESIF/CORALLIA 1 x PEPR 1 x BPI-France	1 x Industrial 4 x University of Rennes 1 (PI)
Submitted	1 1xMSCA (WPL)	2 2xAgence de Programmes ASIC (PI, WPL)	
Total	13		5

International projects

Submitted	"DREAMS: Driving the Radiation reliability of Emerging AI/ML Solutions"
Position	WokrPachage Leader
Organism	University of Rennes, IRISA, INRIA Centre at Rennes University, France (EUR 400 000)
Funds	European - HORIZON-MSCA
09/2024 - 08/2027	"ARCHYTAS: ARCHitectures based on unconventional accelerators for dependable/energY efficienT AI Systems"
Position	WorkPackage Leader
Organism	University of Rennes, IRISA, INRIA Centre at Rennes University, France (EUR 802 750)
Funds	European - EDF
01/2016 - 12/2019	"ARGO: WCET-Aware Parallelization of Model-Based Applications for Heterogeneous Parallel Systems"
Position	Participant
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France (EUR 568 750)
Funds	European - H2020
01/2012 - 12/2013	"END: Models, Solutions, Methods and Tools for ENergy-Aware Design."
Position	Participant
Organism	University of Patras, Greece

	(EUR 16 688)
Funds	European - ENIAC
01/2009 - 12/2009	"MICROMEDIA: Development of an application specific microelectronics device: from the idea to the product"
Position	Participant
Organism	University of Patras, Greece
Funds	European - Leonardo Da Vinci
01/2010 - 12/2013	"INTERACTIVE: Accident avoidance by active intervention for intelligent Vehicles"
Position	Participant
Organism	Institute of Communications and Computer Systems (ICCS), Greece
	(EUR 1 147 240)
Funds	European - FP7
01/2010 - 12/2012	"MINIFAROS: Low-cost Miniature Laser scanner for Environment Perception"
Position	Participant
Organism	Institute of Communications and Computer Systems (ICCS), Greece
	(EUR 260 442)
Funds	European - FP7

National projects

Submitted	"CHIPMOSAIC: Design chain for a modular architecture of advanced heterogeneous computing systems based on interconnected chiplets"
Position	Principal Investigator
Organism	University of Rennes, IRISA, INRIA Bretagne Atlantique, France
	(EUR 438 000)
Submitted	"COACH: Optimized Design of Complex and Heterogeneous Architectures"
Position	WorkPackage Leader
Organism	University of Rennes, IRISA, INRIA Bretagne Atlantique, France
	(EUR 446 000)
01/2023 - 12/2027	"AdaptingING: Adaptive architectures for embedded artificial INtelliGence"
Position	Participant
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
	(EUR 900 000)
01/2023 - 12/2025	"CYBERPROS: Emulateur de cyberattaques et d'evaluation de la securite des systemes processeurs"
Position	Participant
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
	(EUR 285 000)
Funds	France - BPI France
03/2022 - 08/2025	"FASY: FAult-aware timing behaviour for safety-critical multicore SYstems"
Position	Principal Investigator
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
	(EUR 303 321)
Funds	France - ANR JCJC
01/2022 - 11/2025	"RE-TRUSTING: REliable hardware for TRUSTworthy artificial INtelliGence"
Position	Work-package co-responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France

	(EUR 211 483)
Funds	France - ANR PRCE
11/2017 - 11/2020	"FLODAM: Flot Logiciel de Durcissement aux Fautes des Architectures Multi-Coeurs"
Position	Work-package co-responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
	(EUR 395 950)
Funds	France - RAPID DGA
09/2013 - 08/2014	"TOAST: Time Oriented criticAl SysTems"
Position	Participant
Organism	Office National d'Études et de Recherches Aérospatiales, France
Funds	France - STAE Foundation
11/2010 - 12/2011, 03/2010 - 06/2010	"LOC: Microelectronics for Lab-On-chip molecular analysis systems for genetical and environmental applications"
Position	Work-package co-responsible
Organism	University of Patras, Greece
Funds	Greece - European Structural and Investment Funds (ESIF) - CORALLIA
	(EUR 280 880)

National contracts

2021 - 2023	"Hardware acceleration on reconfigurable FPGA architectures for next-generation edge/cloud infrastructures"
	(EUR 217 289)
Position	Participant
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
Funds	France - Orange labs
2022 - 2023	"DUNE: hardware vulnerability analysis for Deep neUral Networks"
	(EUR 9 600)
Position	Scientific responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
Funds	France - Scientific challenges University of Rennes 1
Collaboration	University of Trento, Italy
2019 - 2020	"RITSA: Run-time Infrastructure for fault Tolerance on Safe-critical multicore Architectures"
	(EUR 7 000)
Position	Scientific responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
Funds	France - Scientific challenges University of Rennes 1
Collaboration	Collins Aerospace, Ireland
2019 - 2020	"Reliable and safe, real-time MEMories"
	(EUR 1 000)
Position	Scientific responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
Funds	France - Research international collaborations University of Rennes1
Collaboration	Aristotle University of Thessaloniki, Greece
2016 - 2017	"Energy MAnagement wireless sensor networks with Quality of Service (QoS)"

	(EUR 1 500)
Position	Scientific responsible
Organism	University of Rennes 1, IRISA, INRIA Bretagne Atlantique, France
Funds	France - Research international collaborations University of Rennes1
Collaboration	University of Patras, Greece

5.6 Collaborations outside the host lab

I have the following main collaborations with universities, research centers and companies:

- International: Lei Mo (Southest University of China, China), Stefanos Skalistis (Collins Aerospace, Irenand), Paolo Rech (University of Trento, Italy), Jose Azambuja (Université fédérale du Rio Grande do Sul, Brazil), Francky Catthoor (IMEC, Belgium), Georgios Keramidas (Aristotle University of Thessaloniki, Greece), Christos Panagiotou (University of Patras, Greece)
- National: Tomasz Kloda (LASS-CNRS, Toulouse), Youri Helen (DGA, Rennes), Julien Galizzi (CNES, Toulouse), Guillaume Hubert and Claire Pagetti (ONERA), Patrice Deroux-Dauphin (TEMENTO), Mathieu Roy (LAAS-CNRS, Toulouse), Christine Rochange (IRIT, Toulouse), Alberto Boisio (INL), Haralampos Stratigopoulos (LIP6)

5.7 Service to the research community

Table 7 summarises my service to the research community. The table lists my participation in PhD defence juries, PhD advisory committees, PhD fellowship committees, organisation of conferences, and technical program committees, and presents my services as an editor and reviewer in international journals and conferences.

TABLE 7: Summary of service to the research community.

	International	**National**
PhD defence jury (*Reviewer)	8	12
Nicolo' Bellarmino, "Computational Intelligence for Computer-Aided Design Machine Learning Techniques for Microcontrollers Performance Screenings", Politecnico di Torino, Italy (2024) **Andreas Kouloumbris**, "Task allocation and scheduling optimization in edge-hub-cloud environments", KIOS, Cyprus (2024) **Matteo Zini***, "Analysis and Mitigation of Memory Contention in Real-Time Embedded Systems" Scuola Superiore Sant'Anna, Italy (2024) **Süleyman Savas**, "Hardware/Software Co-design of Heterogenous Manycore Architectures" Halmstad University, Sweden (2019) **Satyajit Das**,"Architecture and Programming Model Support For Reconfigurable Accelerators in Multi-Core Embedded Systems", University of Bretagne-Sud, Lorient, France & University of Bologna, Italy (2018) **Dimitrios Tsitsipis**, "Security Techniques in Wireless Sensor Networks with Emphasis on Cost Reduction in Key Management Schemes Using Topological Methods", University of Patras, Greece (2018) **Mahdad Davari**, "Advantages Towards Data-Race-Free Cache coherence Through Data Classification", Uppsala University, Sweden (2017) **Sofia Maria Dima**, "Wireless sensor and actuator Networks (WSANS): Event-detection algorithms based on fuzzy logic techniques with extension to real-time constraints", University of Patras, Greece (2016)		
Alban Gruin* "Efficient, Predictable, and Composable Computing Core for Safety-Critical Real-Time Systems", University of Toulouse III, France (2024) **Iban Guinebert** "Methodology for the safe integration of neural networks accelerators", ISAE-SUPAERO, France (2024)		

Ali Piri* “Designing space exploration for precision-minded computing”, INL, France (2024)
Alexis Generes*, “Dynamic Memory Cache Allocation to Ensure Peaceful Coexistence of Tasks with Multiple Criticalities on Multi-Core Systems”, ISAE-SUPAERO, France (2024)
Quentin Dariol*, “Early Timing and Energy Prediction and Optimization of Artificial Neural Networks on Multi-Core Platforms”, University of Nantes, France (2023)
Rémi Meunier*, “Predicting application execution time in multi-core architectures”, INSA Toulouse, France (2023)
Ali Oudhriri*, “Performance of a Neural Network Accelerator Architecture and its Optimization Using a Pipeline-Based Approach”, University of Sorbonne, France (2023)
Guillaume Didier, “Calibration Done Right: Noiseless Flush and Flush Attacks”, ENS Paris, France (2023)
Esteban Perrotin, “Certification and dependability of online detection systems for aeronautics”, University of Toulouse, France (2023)
Jeachul Lee, “Approximate communication techniques exploration for efficient nano-photonics interconnects”, University of Rennes 1, France (2022)
Kleovoulos Kaliatzidis, “Ultra wide-issue superscalar processors”, University of Rennes 1, France (2020)
Aswinkumar Sridharan, “Adaptive and Intelligent Memory Systems”, University of Rennes 1, France (2016)

PhD Advisory committee	-	5

Vincent Fu, “Optimization Strategy for High-Performance Computing Architecture Exploration”, University of Sorbonne, France (2023 - 2024)
Racim Boussa, “A Securing DNN Hardware Accelerators Against Side-Channel Attacks”, INSA Rennes, France (2023 - 2024)
Joel Ako ekissi, “Assessment of the moisture content of cocoa beans using image analysis”, INSA Rennes, France (2023 - 2024)
Kleovoulos Kaliatzidis, “Ultra wide-issue superscalar processors”, University of Rennes 1, France (2016 - 2020)
Gaël Deest, “Compute with errors”, University of Rennes 1, France (2014 - 2016)

PhD fellowship committee	-	7

CORDIS: International PhD fellowships INRIA, Rennes, France (2015-2019)
Moyens Incitatifs: Selection Postdoc, Phd, Ingenieur, INRIA, Rennes, France (2020 - 2021)

Conference organisation	22	2

ECRTS’26: Euromicro Conference on Real-time Systems, Program Chair (Qualis: A2, Core: A)
RTNS’25: International Conference on Real-Time Networks and Systems, Program Chair
ETS’25: IEEE European Test Symposium, Special Session chair (Qualis: B2)
ESWEEK (’25, ’24): IEEE/ADM Embedded system Week, Education chair (Qualis: A1)
DATE’25: IEEE/ADM Design, Automation and Test in Europe, Young People Program: Careers Fair – Academia & University Fair Chair (Qualis: A1)
DDECS’25: IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, Publicity Chair (CORE: B)
IOLTS(’25,’24): IEEE International Symposium on On-Line Testing and Robust System Design, General Chair (Qualis: B1)
ISVLSI’25: IEEE Computer Society Annual Symposium on VLSI, Student Research Forum chair (Qualis: B1)
RTSS’23: IEEE Real-Time Systems Symposium, Hot Topic Day Chair (Qualis: A1)

IOLTS'23: IEEE International Symposium on On-Line Testing and Robust System Design, General Vice Chair (Qualis: B1)
SELSE'23: IEEE Workshop Silicon Errors in Logic – System Effects, Program chair
ETS '24,'23: IEEE European Test Symposium, PhD Forum chair, (Qualis: B2)
ISVLSI'22: IEEE Computer Society Annual Symposium on VLSI, Student Research Forum chair, Computer-Aided Design and Verification chair (Qualis: B1)
RTAS ('22, '23): IEEE Real-Time and Embedded Technology and Applications Symposium, Brief Presentation chair (Qualis: A2, Core: A)
ECRTS ('21, '22): Euromicro Conference on Real-Time Systems, Artifact Evaluation chair (Qualis: A2, Core: A)
ARC'21: International Symposium on Applied Reconfigurable Computing, Publicity and Web chair (Qualis: B3)
ISVLSI'20: IEEE Computer Society Annual Symposium on VLSI, Publication chair (Qualis: B1)
JSI'22: INRIA Scientific Days Organisation committee
TORRENTS'13: Workshop Time ORiented Reliable Embedded NeTworked Systems, Assistant

Conference Jury	2	-
DATE'24: IEEE/ADM Design, Automation and Test in Europe, University Fair Jury (Qualis: A1) **ITC'24:** International Test Conference, Academic jury of McCluskey Doctoral Thesis Award (Qualis: A1)		

Conference session chairing	15	1
TPTR'24: IEEE Top Picks in Test and Reliability **DATE'24:** IEEE/ADM Design, Automation and Test in Europe (Qualis: A1) **RTSS'23:** IEEE Real-Time Systems Symposium, Hot Topic Day Chair (Qualis: A1) **ECRTS'23:** Euromicro Conference on Real-time Systems (Qualis: A2, Core: A) **ETS ('23,'24):** IEEE European Test Symposium (Qualis: B1) **IOLTS ('24, '23, '22):** IEEE International Symposium on On-Line Testing and Robust System Design (Qualis: B1) **ISVLSI'22:** IEEE Computer Society Annual Symposium on VLSI (Qualis: B1) **RTAS'22:** IEEE Real-Time and Embedded Technology and Applications Symposium (Qualis: A2, Core: A) **DATE'22:** IEEE/ACM Design, Automation and Test in Europe (Qualis: A1) **SELSE ('23, '22):** IEEE Workshop on Silicon Errors in Logic – System Effects **ARC'21:** International Symposium on Applied Reconfigurable Computing, Publicity and Web chair (Qualis: B3) **JSI'22:** INRIA Scientific Days		

Technical Program Committee	66	4
DAC ('25, '24, outstanding TPC member award): Design Automation Conference (Qualis: A1) **DAC-LBR ('24):** Design Automation Conference - Late Breaking Results (Qualis: A1) **RTSS ('23, '22, '21):** IEEE Real-Time Systems Symposium (Qualis: A1, Core: A*) **DATE ('24, '23, '22, '21, '20):** Design, Automation and Test in Europe (Qualis: A1) **EMSOFT ('24, '23):** ACM/IEEE International Conference on Embedded Software (Qualis: A2) **EMSOFT-LBR ('24):** ACM/IEEE International Conference on Embedded Software (Qualis: A2) **CASES '24:** International Conference on Compilers Architecture and Synthesis for Embedded Systems (Qualis: A2) **ECRTS ('25, '23, '22, '21, '20, '19):** Euromicro Conference on Real-time Systems (Qualis: A2, Core: A)		

RTAS ('25,'24, '23, '21, '20, '19): Real-time and Embedded Technology and Applications Symposium (Qualis: A2, Core: A)
VLSID ('25): International Conference on VLSI design (Qualis: A2, Core: A)
RTCSA ('25, '24, '23): IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (Qualis: B1, Core: B)
ICPADS '23: IEEE International Conference on Parallel and Distributed Systems (Qualis: B1)
ISVLSI ('25, '24, '23, '22): IEEE Computer Society Annual Symposium on VLSI (Qualis: B1)
ETS ('25, '24, '23): IEEE European Test Symposium (Qualis: B2)
SAMOS ('24, '23, '22, '21, '20, '19): Int. Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (Qualis: B2)
DS-RT ('24, '23, '22): International Symposium on Distributed Simulation and Real Time Applications (Qualis: B2)
LATS ('25): IEEE Latin American Test Symposium
AEiC ('25): Ada-Europe International Conference on Reliable Software Technologies (Qualis: B2)
OSPERT ('25): Operating Systems Platforms for Embedded Real-Time applications
IISWC'20: IEEE International Conference on Workload Characterization (CORE: B)
HPCC ('21, '20): IEEE International Conference on High Performance Computing and Communications (CORE: B)
ARC ('24, '23, '22, '21): International Symposium on Applied Reconfigurable Computing (Qualis: B3)
NPC'22: International Conference on Network and Parallel Computing (Qualis: B3)
CPSCom ('22,'21): IEEE International Conference on Cyber, Physical and Social Computing (Qualis: B4)
RTNS ('23, '22): International Conference on Real-Time Networks and Systems
SELSE'23: IEEE Workshop Silicon Errors in Logic – System Effects
AI-TREATS'24: Workshop on AI Hardware: Test, Reliability and Security
JRWRTC'16: Junior Researcher Workshop on Real-time Computing
COMPAS ('24, '23, '22, '21): Conférence francophone d'informatique en Parallélisme, Architecture et Système

Research group animator	-	5
GdR-SOC2'23-'27: Research group on System-on-Chip, Embedded Systems and Connected Systems, Scientific axis of High Performance Embedded Computing		

Journal editor	6	-
JSA: Journal of Systems Architecture, Elsevier, (SJR: Q1) (Associate Editor, since 2023)		
MICROP: Microprocessors and Microsystems, Elsevier, (SJR: Q3) (Handling editor, since 2023)		
JPDP: Elsevier Journal of Parallel and Distributed Computing, "Parallel and Distributed Computing for Cyber-Physical Systems" (SJR: Q2) (Special Issue, 2021)		
MICROP: Microprocessors and Microsystems, Elsevier, "Holistic Technologies for Sustainable Cyber-Physical Systems" (SJR: Q3) (Special Issue, 2020)		
JSPE: Journal of Software: Practice and Experience, Wiley Press, "Software and Hardware Co-Design for Sustainable Cyber-Physical Systems", (SJR: Q2) (Special Issue, 2020)		
CSEE JPES: CSEE Journal of Power and Energy Systems, "Cyber-Physical System Technologies for Sustainable Power and Energy Systems", (Special Issue, 2020)		

Journal review	27	-
CSR: Elsevier Computer Science Review (since 2024, SJR: Q1)		
D&T: IEEE Design and Test (since 2024, SJR: Q2-3)		

TPDS: IEEE Transactions on Parallel and Distributed Systems (since 2023, SJR: Q1)
CS: ACM Computing Surveys (since 2023, SJR: Q1)
JRR: Journal of Risk and Reliability (since 2023, SJR: Q2)
TII: IEEE Transactions on Industrial Informatics (since 2022, SJR: Q1)
RTS: Springer Real-Time systems (since 2022, SJR: Q2)
CN: Elsevier Computer Networks (since 2022, SJR: Q1)
TNSM: IEEE Transactions on Network and Service Management (since 2021, SJR: Q1)
TSUSC: IEEE Transactions on sustainable computing (since 2021, SJR: Q1)
JETC: ACM Journal on Emerging Technologies in Computing Systems (since 2021, SJR: Q2)
TECS: ACM Transactions on embedded computing Systems (since 2021, SJR: Q2)
TASE: IEEE Transactions on Automation Science and Engineering (since 2020, SJR: Q1)
JSS: Elsevier Journal of Systems & Software (since 2020, SJR: Q2)
MIS: Hindawi Mobile Information systems (since 2020, SJR: Q2)
JIOT: IEEE Journal of Internet of Things (since 2019, SJR: Q1)
JKSUCIS: Elsevier Journal of King Saud University - Computer and Information Sciences (since 2019, SJR: Q2)
TODAES: ACM Transactions on Design Automation of Electronic Systems (since 2019, SJR: Q2)
JETT: Journal Electronic Testing (since 2024, SJR: Q3)
JSPE: Wiley Journal of Software: Practice and Experience (since 2019, SJR: Q2)
JSEP: Wiley Journal of Software: Evolution and Process (since 2019, SJR: Q3)
MICROP: Elsevier Microprocessors and microsystems (since 2019, SJR: Q3)
TCAD: IEEE Transactions on Computer-Aided Design of Intergrated Circuits and Systems (since 2018, SJR: Q2)
IEEE Access: (since 2017, SJR: Q1)
TETC: IEEE Transactions on Emerging Topics in Computing (since 2016, SJR: Q1-Q2)
TVLSI: IEEE Transactions on Very Large Scale Intergration (since 2015, SJR: Q1-Q2)
TC: IEEE Transactions on Computers (since 2011, SJR: Q1)

Additional external conference review	12	-

ICCAD ('21, '22): IEEE/ACM International Conference On Computer Aided Design (Qualis: A1)
DAC ('20, '19): Design Automation Conference (Qualis: A1)
FPL'15: Field-Programmable Logic and applications (Qualis: A2)
CF'18: ACM International Conference on Computing Frontiers (Qualis: B1)
IECON'15: IEEE Industrial Electronics Society (Qualis: B1)
PATMOS ('13, '12, '11, '10, '09): Int. Conference on Power and Timing Modeling, Optimization and Simulation (Qualis: B2)

Invited talks	2	5

"Reliability analysis and protection of RISC-V processors for critical embedded systems", BITFLIP, European CyberWeek, France, 2023
"Run-time adaptation of task execution in time-critical systems: Challenges and Solutions", International workshop sCalable and PrecIse Timing AnaLysis for multiocre platforms (CAPITAL), Virtual event, 2021
"Reliability analysis and protection for AI critical embedded systems", X-GDR BarCamp on AI Implementation Challenges - Security, Reliability, Sustainability and New Technologies, GDR SOC2, France, 2023
"Energy-Quality-Time Optimized Mapping for Imprecise Computation Tasks on Multicores", GDR RO and SOC2, France, 2022

"Scalable and Near-optimal Design Space Exploration methodologies for loop dominated embedded systems", Microprocessors and digital systems lab, National Technological University of Athens, Athens, Greece, 2013 and ONERA, Toulouse, France, 2014

Popularisation	-	2
INRIA Emergencies, "Rethinking Hardware Reliability for Trustworthy AI"		
INRIA Emergencies, "Harden multi-cores against ionizing radiation"		

5.8 List of publications

(*: Supervision, +: Main contributor, -: Minor contributor)

Patent

2010

[P1] P. Raghavan, D. Novo Bruna, F. Catthoor and A. Kritikakou (+), "Method and Device for Reducing Power Consumption in Application Specific Instruction Set Processors", US Patent Application No: 2011/055836, Aug., 2010

Scientific Books

2014

[B2] A. Kritikakou (+), F. Catthoor and C. Goutis, "Scalable and near-optimal design space exploration for embedded systems", Springer, 2014

2010

[B1] F. Catthoor, P. Raghavan, M. Jayapala, A. Kritikakou (+) and J. Absar, "Ultra-Low Power Domain Specific Instruction Set Processors", Springer, 2010

Scientific book chapters

2018

[BC2] L. Mo, A. Kritikakou (*) and O. Sentieys, "Imprecise Computation Task Mapping on Multi-Core Wireless Sensor Networks", Encyclopedia of Wireless Netwroks, Springer, 2018

2010

[BC1] H. Michail, A. Gregoriades, V. Kelefouras, G. Athanasiou, A. Kritikakou (-) and C. Goutis, "Authentication with RIPEMD-160 and other alternatives: A Hardware Design Perspective", New Advanced Technologies, IN-TECH Inc. Publishers, Vienna, Austria, pp. 103-124.

International Journals

2024

[J35] IF: 5.1 SJR: Q1 F. dos Santos, N. Cavagnero, M. Ciccone, G. Averta, A. Kritikakou (*), O. Sentieys, P. Rech and T. Tommasi. "Improving Deep Neural Network Reliability via Transient-Fault-Aware Design and Training". IEEE Transactions on Emerging Topics in Computing, 2024

[J34] IF: 5.883 SJR: Q1 L. Mo, X. Li, A. Kritikakou (*) and X. Zhai, "Contention and Reliability-Aware Energy Efficiency Task Mapping on NoC-Based MPSoCs", IEEE Transactions on Reliability, 2024

[J33] IF: 1.679 SJR: Q2
M. Traiola, F. F. dos Santos, O. Sentieys and A. Kritikakou (*), "Impact of High-Level-Synthesis on Reliability of Artificial Neural Network Hardware Accelerators", IEEE Transactions on Nuclear Science, 2024.

[J32] IF: 1.679 SJR: Q2
P. Bodmann, M. Saveriano, A. Kritikakou (-) and P. Rech, "Neutrons Sensitivity of Deep Reinforcement Learning Policies on EdgeAI Accelerators", IEEE Transactions on Nuclear Science, 2024.

2023

[J31] IF: 3.691 SJR: Q1
L. Mo, X. Li, A. Kritikakou (*) and P. You, "Optimal IC Task Mapping to Maximize QoS on Heterogeneous Multicore Systems", IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II), 2023

[J30] IF: 2.273 SJR: Q1
L. Mo, Q. Zhou, A. Kritikakou (*) and X. Cao, "Energy Optimized Task Mapping for Reliable and Real-Time Networked Systems", ACM Transactions on Sensor Networks (TOSN), 2023

[J29] IF: 3.746 SJR: Q1
M. Cui, A. Kritikakou (*), L. Mo, and E. Casseau, "Near-optimal Energy-Efficient Partial-Duplication Mapping of Real-Time Parallel Applications ", Elsevier Journal of System Architecture (JSA), 2023

[J28] IF: 2.807 SJR: Q2
A. Kritikakou (+) and S. Skalistis, "Mitigating Mode-Switch through Run-time Computation of Response Time", ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023

2022

[J27] IF: 2.273 SJR: Q1
X. Li, L. Mo, A. Kritikakou (*) and O. Sentieys, "Approximation-aware Task Deployment on Heterogeneous Multi-core Platforms with DVFS", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2022

[J26] IF: 1.679 SJR: Q2
F. dos Santos, A. Kritikakou (*), J.E. Rodriguez Condia, J.D. Guerrero-Balaguera M. Sonza Reorda, O. Sentieys, and P. Rech, "Characterizing a Neutron-Induced Fault Model for Deep Neural Networks", IEEE Transactions on Nuclear Science (TNS), 2022

[J25] IF: 1.161 SJR: Q3
R. Psiakis, A. Kritikakou (*) and O. Sentieys, "Dynamic Fault-Tolerant VLIW Processor with Heterogeneous Function Units", Elsevier Microprocessors and Microsystems (MICPRO), 2022

[J24] IF: 1.244 SJR: Q3
M. Cui, A. Kritikakou (*), L. Mo, and E. Casseau, "Energy-aware Partial-Duplication Task Mapping under Real-Time and Reliability Constraints for multiple DVFS schemes", Springer International Journal of Parallel Programming (IJPP), 2022

2021

[J23] IF: 2.402 SJR: Q1
R. Mercier, C. Killien, A. Kritikakou (*), Y. Helen, and D. Chillet, "BiSuT: A NoC-Based Bit-Shuffling Technique for Multiple Permanent Faults Mitigation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2021

[J22] IF:11.705 SJR: Q1
L. Mo, A.Kritikakou (*), O. Sentieys, and X. Cao, "Real-time Imprecise Computation Tasks Mapping for DVFS-Enabled Networked Systems" IEEE Journal of Internet of Things (IEEE JIOT), 2021

2020

[J21] IF: 8.960 SJR: Q1
A.Kritikakou (+), R. Psiakis, F. Catthoor, and O. Sentieys, "Binary Tree Classification of Rigid Error Detection and Correction Techniques" Journal of ACM Computed Surveys (ACM CS), 2020

2019

[J20] IF: 5.430 SJR: Q1
L. Mo, X. Cao and A. Kritikakou (*), "Event-Driven Joint Mobile Actuators Scheduling and Control in Cyber-Physical Systems",IEEE Transaction on Industrial Informatics (IEEE TII), 2019

[J19] IF: 5.863 SJR: Q1
L. Mo, A.Kritikakou (*), and S. He, "Energy-aware Multiple Mobile Chargers Coordination for Wireless Rechargeable Sensor Networks", IEEE Journal of Internet of Things (IEEE JIOT), 2019

[J18] IF: 1.514 SJR: Q2
L. Mo, and A.Kritikakou (*), "Mapping Imprecise Computation Tasks on Cyber-Physical Systems", Springer Peer-to-Peer Networking and Applications (Springer P2PNA), 2019

2018

[J17] IF: 5.863 SJR: Q1
L. Mo, X. Cao, Y. Song and A.Kritikakou (*), "Distributed Node Coordination for Real-Time Energy-Constrained Control in Wireless Sensor and Actuator Networks", IEEE Journal of Internet of Things (IEEE JIOT), 2018

[J16] IF: 3.218 SJR: Q1
L. Mo, A. Kritikakou (*) and O. Sentieys, "Controllable QoS for Imprecise Computation Tasks on DVFS Multicores with Time and Energy Constraints", IEEE Journal on Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS), 2018

[J15] IF: 2.089 SJR: Q2
L. Mo, A. Kritikakou (*) and O. Sentieys, "Energy-Quality-Time Optimized Task Mapping for DVFS-enabled Real-Time Multicore", IEEE Transaction on Computer Aided Design (IEEE TCAD), 2018

[J14] IF: 0.870 SJR: Q3
A. Kritikakou (+), T. Marty and M. Roy, "DYNASCORE: DYNAmic Software COntroller to Increase REsource Utilization in Mixed-Critical Systems", ACM Trans. Design Automation of Electronic Systems (ACM TODAES), Vol. 23, Issue 2, Jan., 2018

2016

[J13] IF: 1.326 SJR: Q2
V. Kelefouras, A. Kritikakou (-), I. Mporas and V. Kolonias, "A High Performance Matrix-Matrix Multiplication Methodology for CPU and GPU Architectures", Journal of Supercomputing (JS), Springer, Jan, 2016

[J12] IF: 0.850 SJR: Q3
A.Kritikakou (+), F. Catthoor, V. Kelefouras and C. Goutis, "Array Size Computation under Uniform Overlapping & Irregular Accesses", ACM Trans. Design Automation of Electronic Systems (ACM TODAES), Jan, 2016

2015

[J11] IF: 1.088 SJR: Q2
V.I. Kelefouras, E. Papadima, A. Kritikakou (+) and C.E. Goutis, "A Methodology for Speeding up Matrix Vector Multiplication for single/multi-core architectures", Journal of Supercomputing (JS), Springer, Mar, 2015

[J10] IF: 0.556 SJR: Q4
V.I. Kelefouras, A. Kritikakou (+) and C.E. Goutis, "A Methodology for Speeding up Loop Kernels by Exploiting the Software Information and the Memory Architecture", Journal of Computer Languages, Systems and Structure (COMLAN), Feb, 2015

2014

[J9] IF: 0.917 SJR: Q2
V.I. Kelefouras, A. Kritikakou (+) and C.E. Goutis, "A Matrix Matrix Multiplication Methodology for single/multi-core architectures using SIMD", Journal of Supercomputing (JS), Springer, Jan, 2014

[J8] IF: 0.824 SJR: Q2
A.Kritikakou (+), F. Catthoor, V. Kelefouras and C. Goutis, "A Scalable & Near-optimal Representation of Access Schemes for Memory Management", ACM Trans. Architecture and Code Optimization (ACM TACO), Vol. 11, No. 1, Feb, 2014

2013

[J7] IF: 4.043 SJR: Q1
A.Kritikakou (+), F. Catthoor, V. Kelefouras and C. Goutis, "A Systematic Approach to Classify Design Time Global Scheduling Techniques", ACM Computing Surveys (ACM CS), 2013, Vol. 45, No. 2

[J6] IF: 0.597 SJR: Q3
A.Kritikakou (+), F. Catthoor, G.S. Athanasiou, V. Kelefouras and C. Goutis, "Near-optimal Microprocessor & Accelerators Co-Design with Latency & Throughput Constraints", ACM Trans. Architecture and Code Optimization (ACM TACO), Vol.10, No.2, May, 2013

[J5] IF: 0.520 SJR: Q2
A.Kritikakou (+), F. Catthoor, V. Kelefouras and C. Goutis, "Near-optimal & Scalable Intra-signal In-place for Non-overlapping & Irregular Access Scheme", ACM Trans. Design Automation of Electronic Systems (ACM TODAES), Vo. 19, no. 1, Dec, 2013

[J4] IF: 0.564 SJR: Q3
V.I. Kelefouras, A. Kritikakou (-), C.E. Goutis and Costas Siourounis, "A Methodology for speeding up MVM for regular, Toeplitz and Bisymmetric Toeplitz matrices", Journal of Signal Processing Systems (JSPS), Springer, 2013, pp. 1-15

[J3] IF: 0.841 SJR: Q3
V.I. Kelefouras, A. Kritikakou (+) and C.E. Goutis, "A Methodology for Speeding Up Edge and Line Detection Algorithms focusing on Memory Architecture Utilization", Journal of Supercomputing (JS), Springer, Dec, 2013

2012

[J2] IF: 0.917 SJR: Q3
N. Alachiotis, V. Kelefouras, G. Athanasiou, H. Michail, A. Kritikakou (-) and C. Goutis, "A Data Locality Methodology for Matrix-Matrix Multiplication Algorithm", Journal of Supercomputing (JS), Springer, 2012, Vol. 59, No. 2, pp. 830-851

2011

[J1] IF: 2.628 SJR: Q1
V.I. Kelefouras, G.S. Athanasiou, N. Alachiotis, H. E. Michail, A. Kritikakou (-) and C.E. Goutis, "A Methodology for Speeding Up Fast Fourier Transform Focusing on Memory Architecture Utilization", IEEE Transactions on Signal Processing (IEEE TSP), 2011, Vol.59, No. 12, pp. 6217-6226

International Conferences

Conference papers with proceedings

2024

[C48] Qualis: A1
L. Roquet, F. Santos, P. Rech, M. Traiola, O. Sentieys and A. Kritikakou (*), "Cross-Layer Reliability Evaluation and Efficient Hardening of Large Vision Transformers Models", ACM/EDAC/IEEE Design Automation Conference (DAC), 2024.

[C47] Qualis: A1
W. Guilleme, A. Kritikakou (*), Y. Helen, D. Chillet and C. Killian, "HTAG-eNN: Hardening Technique with AND Gates for Embedded Neural Networks", ACM/EDAC/IEEE Design Automation Conference (DAC), 2024.

[C46] Qualis: A2
M. Ahmadilivani, A. Bosio, B. Deveautour, F. dos Santos, J.D. Guerrero-Balaguera, M. Jenihhin, A. Kritikakou (-), R. Limas Sierra, S. Pappalardo, J. Raik, J.E. Rodriguez Condia, M. Sonza Reorda, M. Taheri, and M. Traiola, "Reliability Assessment Recipes for DNN Accelerators", Special Session, IEEE VLSI Test Symposium (VTS), 2024.

[C45] Qualis: A2
R. Nikiema, M. Traiola, and A. Kritikakou (*), "Compiler impact on reliability assessment for RISC-V processors", Special Session, IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2024.

[C44] Qualis: B1
F. dos Santos, M. Traiola, and A. Kritikakou (+), "Combining Fault Simulation and Beam Data for CNN Error Rate Estimation on RISC-V Commercial Platforms", IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2024

[C43] Qualis: B1
W. Guilleme, A. Kritikakou (*), Y. Helen, D. Chillet and C. Killian, "VANDOR: Mitigating SEUs into Quantized Neural Networks", IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2024

[EC1] Qualis: B2
D. Gnad, M. Gotthard, J. Krautter, A. Kritikakou (-), V. Meyers, P. Rech, J.E. Rodriguez Condia, A. Ruospo, E. Sanchez, F.F. dos Santos, O. Sentieys, M. Tahoori, R. Tessier, and M. Traiola, "Reliability and Security of AI Hardware", Special Session, IEEE European Test Symposium (ETS), 2024

[C41] Qualis: B3
J. Chen, G. Esposito, F. dos Santos, J.D. Guerrero-Balaguera, A. Kritikakou (-), M. Krstic, R. Limas, J.R. Condia, M. Sonza Reorda, M. Traiola, and A. Veronessi "Reliability Assessment of Large DNN Models: Trading Off Performance and Accuracy", Special Session, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2024

[C40] Qualis: B3
L. Roquet, F. Santos, P. Rech, M. Traiola, O. Sentieys and A. Kritikakou (*), " MaxiMals: A Low-cost Hardening Technique for Large Vision Transformers", European Conference on Radiation and its Effects on Components and Systems (RADECS), 2024.

[C39]
S. Lee, E. Casseau, A. Kritikakou (*), O. Sentieys, R. Salvador and J. Galizzi, "On-board Payload Data Processing Combined with the Roofline Model for Hardware/Software Design", IEEE Aerospace Conference (AeroConf), 2024.

2023

[C38] Qualis: A1
R.P. Nikiema, A. Kritikakou (*), M. Traiola and O. Sentieys, "Design with low complexity fine-grained Dual CoreLock-Step (DCLS) RISC-V processors", Special Session, IEEE/IFIP International Conference on Dependable Systems and Networks, Supplementary material (DSN-S), 2023.

[C37] Qualis: A1
M. Traiola, A. Kritikakou (+), and O. Sentieys, "A machine-learning-guided framework for fault-tolerant DNNs", Extended abstract, Design, Automation & Test in Europe (DATE), 2023

[C36] Qualis: A2 Core: A
R.P. Nikiema, A. Kritikakou (*), M. Traiola and O. Sentieys, "Impact of transient faults on timing behavior and mitigation with near-zero WCET overhead", Euromicro Conference on Real-Time Systems (ECRTS), 2023.

[C35] Qualis: B1
R.P. Nikiema, A. Palumbo, A. Aasma, L. Cassano, A. Kritikakou (*), A. Kulmala, J. Lukkarila, M. Ottavi, R. Psiakis, and M. Traiola, "Towards dependable RISC-V cores for edge computing devices", Special Session, IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2023.

[C34] Qualis: B2
M. Traiola, A. Kritikakou (+), and O. Sentieys, "harDNNing: a machine-learning-based framework for fault tolerance assessment and protection of DNNs", IEEE European Test Symposium (ETS), 2023

[C33] Qualis: B3
W. Guilleme, Y. Helen, R. Priem, A. Kritikakou (*), D. Chillet, and C. Killian, "Hardening a Neural Network on FPGA through Selective Triplication and Training Optimization", European Conference on Radiation and its Effects on Components and Systems (RADECS) , 2023.

[C32] Qualis: B3
F. Santos, P. Rech, A. Kritikakou (*), and O. Sentieys, "Neutron-Induced Error Rate of Vision Transformer Models on GPUs", European Conference on Radiation and its Effects on Components and Systems (RADECS) , 2023.

[C31] Qualis: B3
B. Pablo, M. Saveriano, A. Kritikakou (-), and P. Rech, "Neutrons Sensitivity of Deep Reinforcement Learning Policies on EdgeAI Accelerators", European Conference on Radiation and its Effects on Components and Systems (RADECS), 2023.

[C30]
S. Lee, R. Salvador, A. Kritikakou (*), O. Sentieys, J. Galizzi and E. Casseau, "High-Level Synthesis (HLS)-Based On-board Payload Data Processing considering the Roofline Model", European Data Handling & Data Processing Conference (EDHPC), 2023.

2022

[C29] Qualis: A1
A. Kritikakou (+), O. Sentieys, G. Hubert, Y. Helen, J.F. Coulon, and P. Deroux-Dauphin, "FLODAM: Cross-layer fault-tolerant reliability analysis flow for complex hardware designs", Multi-Partner Project Session, Design, Automation & Test in Europe (DATE), 2022

[C28] Qualis: A1
L. Mo, Q. Zhou, A. Kritikakou (*), and J. Liu, "Energy Efficient, Real-time and Reliable Task Deployment on NoC-based Multicores with DVFS", Design, Automation & Test in Europe (DATE), 2022

[C27] Qualis: B1
A. Kritikakou (+), P. Nikolaou, I. Rodriguez-Ferrandez, J. Paturel, L. Kosmidis, M.K. Michael, O. Sentieys, D. Steenari, "Functional and Timing Implications of Transient Faults in Critical Systems", Special Session, IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2022

[C26] Qualis: B1
F.F. dos Santos, A. Kritikakou (*), and O. Sentieys, "Experimental evaluation of neutron-induced errors on a multicore RISC-V platform", IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2022

[C25] Qualis: B4
I. Krayem, R. Mercier, C. Killian, A. Kritikakou (*), and D. Chillet, "Data and Fault Aware Routing Algorithm for NoC Based Approximate Computing", ACM Symposium on Nanoscale Architectures (NANOARCH), 2022

2021

[C24] Qualis: A2 Core: A
M. Cui, A. Kritikakou (*), L. Mo, and E. Casseau, "Fault-Tolerant Mapping of Real-Time Parallel Applications under multiple DVFS schemes", IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 18-21 May, 2021, Virtual conference

[C23] Qualis: B1
R. Mercier, C. Killian, A. Kritikakou (*), Y. Helen and D. Chillet, "A Region-Based Bit-Shuffling Approach Trading Hardware Cost and Fault Mitigation Efficiency", IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2021, Virtual conference

2020

[C22] Qualis: A2
R. Mercier, C. Killien, A. Kritikakou (*), Y. Helen, and D. Chillet, "Multiple Permanent Faults Mitigation through Bit-Shuffling for Network-on-Chip Architecture", International Conference on Computer Design (ICCD), 2020

[C21] Qualis: A2 Core: A
S. Skalistis and A. Kritikakou (+), "Dynamic interference-sensitive run-time adaptation of Time-Triggered schedules", Euromicro Conference on Real-Time Systems (ECRTS), 2020

[C20] Qualis: B1
J. Paturel, A. Kritikakou (*), and O. Sentieys, "Fast Cross-Layer Vulnerability Analysis of Complex Hardware Designs", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 6-8 July, 2020, Limassol, Cyprus

[C19] Qualis: B2
M. Cui, L. Mo, A. Kritikakou (*), and E. Casseau, "Energy-aware Partial-Duplication Task Mapping under Real-Time and Reliability Constraints", International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 5-9 July, 2020, Samos, Greece

2019

[C18] Qualis: A1 Core: A*
S. Skalistis and A. Kritikakou (+), "Timely Fine-grained interference-sensitive runtime adaptation of time-triggered schedules", IEEE Real-Time Systems Symposium (RTSS), 2019

[C17] Qualis: A1
R. Psiakis, A. Kritikakou (*) and O. Sentieys, "Fine-grained Hardware Mitigation for Multiple Long-Duration Transients on VLIW Function Units", Design, Automation & Test in Europe (DATE), 25-29 March, 2019, Florence, Italy

[C16] Qualis: A1
L. Mo, A. Kritikakou (*) and O. Sentieys, "Approximation-aware Task Deployment on Asymmetric Multicore Processors", Design, Automation & Test in Europe (DATE), 25-29 March, 2019, Florence, Italy

[C15]
R.Psiakis, A. Kritikakou (*), E. Casseau and O. Sentieys, "Run-Time Coarse-Grained Hardware Mitigation for Multiple Faults on VLIW Processors", Conference on Design and Architectures for Signal and Image Processing (DASIP), 16-18 October, 2019, Montreal, Canada

2018

[C14] Qualis: B1 Core: B
L. Mo, A. Kritikakou (*), X. Cao, "Collaborative State Estimation and Actuator Scheduling for Cyber-Physical Systems under Random Multiple Events", International Conference on Ad Hoc Networks and Wireless (AdHoc-Now), 5-7 September, 2018, St-Malo, France

2017

[C13] Qualis: A1
S. Derrien, I. Puaut, P. Alefragis, M. Bednaraz, H. Bucherx, C. David, Y. Debray, U. Durak,I. Fassi, C. Ferdinand, D. Hardy, A. Kritikakou (-), G. Rauwerda, S. Reder, M. Sicks,, T. Stripf, K. Sunesen, T. Braak, N. Voros, J. Becker, "WCET-Aware Parallelization of Model-Based Applications for Multi-Cores: the ARGO Approach", Multi-Partner Project Session, Design, Automation & Test in Europe (DATE), 27-31 March 2017, Lausanne, Swiss

[C12] Qualis: A2
L. Mo, A. Kritikakou (*) and O. Sentieys, "Decomposed Task Mapping to Maximize QoS in Energy-Constrained Real-Time Multicores", International Conference on Computer Design (ICCD), 5-8 November, 2017, Massachusetts, USA

[C11] Qualis: B1
R.Psiakis, A. Kritikakou (*), and O. Sentieys, "NEDA: NOP Exploitation with Dependency Awareness for Reliable VLIW Processors", Computer Society Annual Symposium on VLSI (ISVLSI), July 3-5, 2017, Bochum, Germany

[C10] Qualis: B4
R.Psiakis, A. Kritikakou (*), and O. Sentieys, "Run-Time Instruction Replication for Permanent and Soft Error Mitigation in VLIW Processors", International New Circuits and Systems Conference (NEWCAS), 25-28 June, 2017 Strasbourg, France

2016

[C9] A. Kritikakou (+), T. Marty, C. Pagetti, C. Rochange, Michael Lauer and M. Roy, "Multiplexing Adaptive with Classic AUTOSAR? Adaptive Software Control to Increase Resource Utilization in Mixed-Critical Systems", Critical Automotive applications: Robustness & Safety (CARS), Sep 2016, Göteborg, Sweden

2014

[C8] A. Kritikakou (+), O. Baldellon, C. Pagetti, C. Rochange and M. Roy, "Run-time Control to Increase Task Parallelism in Mixed-Critical Workloads", Euromicro Conference on Real-Time Systems (ECRTS), 8-11 July 2014, Madrid, Spain
Qualis: A2
Core: A

[C7] A. Kritikakou (+), C. Pagetti, C. Rochange, M. Roy, Madeleine Faugère, Sylvain Girbal and Daniel Gracia Pérez, "Distributed run-time WCET controller for concurrent critical tasks in mixed-critical systems", International Conference on Real-Time Networks and Systems (RTNS), 8-10 October, 2014, Versailles, France

2012

[C6] D. Tsitsipis, S.M. Dima, A.Kritikakou (+), C. Panagiotou, J. Gialelis, H. Michail and S.Koubias, "Priority Handling Aggregation Technique (PHAT) for Wireless Sensor Networks", International Conference Emerging Technologies and Factory Automation (ETFA),17-21 Sep 2012, Cracow, Poland
Qualis: B1

[C5] A. Kritikakou (+), F.Catthoor, G.S. Athanasiou, V. Kelefouras and C. Goutis, "A Template-based Methodology for Efficient Microprocessor and FPGA Accelerator Co-Design", International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 16-19 July 2012, Samos, Greece
Qualis: B2

[C4] D. Tsitsipis, S.M. Dima, A.Kritikakou (+), C. Panagiotou, and S.Koubias, "Segmentation and Reassembly Data Merge (SaRDaM) Technique for Wireless Sensor Networks", International International on Industrial Technology (ICIT), 19-21 Mar 2012, Athens, Greece
Qualis: B3

2011

[C3] D. Tsitsipis, S.M. Dima, A.Kritikakou (+), C. Panagiotou, and S.Koubias, "Data Merge: A data aggregation technique for Wireless Sensor Networks", Proc. International Conference Emerging Technologies and Factory Automation (ETFA), 5-9 Sep 2011, Toulouse, France
Qualis: B1

2010

[C2] D. Novo, A. Kritikakou (+), P. Raghavan, V.P. Liesbet, H. Jos and F. Catthoor, "Ultra Low Energy Domain Specific Instruction-set Processor for On-line Surveillance", IEEE Symposium on Application Specific Processors (SASP), 13-14 June 2010, Anaheim, CA, USA
Qualis: B4

[C1] H. Michail, A. Gregoriades, V. Papadopoulou, G. Athanasiou, A. Kritikakou (-) and C. Goutis, "Ultra high speed SHA-256 hashing cryptographic module for IPSec hardware/software codesign", International Conference on Security and Cryptography (SECRYPT), 26-28 July 2010, Athens, Greece.
Qualis: B4
Core: B

Work in Progress with proceedings

2020

[W2] A. Kritikakou (+), and S. Skalistis, "Progress-aware dynamic slack exploitation in mixed-critical systems", WiP in Proc. International Conference on Embedded Software (EMSOFT), 20-25 Sep 2020, Virtual Conference
Qualis: A2
Core: A

2013

[W1] Qualis: A1 Core: A*

A. Kritikakou (+), O. Baldellon, C. Pagetti, C. Rochange, M. Roy, and F. Vargas, "Monitoring On-line Timing Information to Support Mixed-Critical Workloads", WiP in Proc. International Conference Real-Time Systems Symposium (RTSS), 3-6 Dec 2013, Vancouver, Canada

Educational Classes with proceedings

2024

[EC1] Qualis: A2 Core: A

M. Traiola, A. Kritikakou (+), S.-I. Filip, O. Sentieys, "Efficient Neural Networks: from SW optimization to specialized HW accelerators", Embedded System Week (ESWEEK), CASES, 2024

Posters and Oral Presentations (including 2.0 publication model)

2024

[PP16] A. Kritikakou (+), O. Sentieys, G. Hubert, Y. Helen, and P. Deroux-Dauphin, "Cross-Layer Reliability Analysis Flow for Complex Hardware Designs", Presentation in Top Picks in Reliability and Testing, ITC, San Diego, 2024.

2023

[PP15] R.P. Nikiema, M. Traiola, O. Sentieys and A. Kritikakou (*), "Time-Bounded Error Mitigation through Dual-Core Lockstep RISC-V using HLS", Poster in RISC-V Summit Europe, Barcelona, 2023.

[PP14] F. F. dos Santos, A. Kritikakou (*), and O. Sentieys, "Reliability evaluation of Convolutional Neural Network's basic operations on a RISC-V processor", Presentation in IEEE Workshop on AI Hardware: Test, Reliability and Security (AI-TREATS), Venice, 2023.

[PP13] M. Traiola, F. F. dos Santos, O. Sentieys and A. Kritikakou (*), "Impact of High-Level-Synthesis on Reliability of Neural Network Hardware Accelerators", Presentation in IEEE Workshop on AI Hardware: Test, Reliability and Security (AI-TREATS), Venice, 2023.

[PP12] F. F. dos Santos, A. Kritikakou (*), and O. Sentieys, "Reliability evaluation of Convolutional Neural Network's basic operations on a RISC-V processor", Presentation in IEEE Nuclear and Space Radiation Effects Conference (NSREC), Kansas City, 2023.

[PP11] M. Traiola, F. F. dos Santos, O. Sentieys and A. Kritikakou (*), "Impact of High-Level-Synthesis on Reliability of Neural Network Hardware Accelerators", Presentation in IEEE Nuclear and Space Radiation Effects Conference (NSREC), Kansas City, 2023.

[PP10] R.P. Nikiema, A. Kritikakou (*), M. Traiola and O. Sentieys, "Design with low complexity fine-grained Dual CoreLock-Step (DCLS) RISC-V processors", Presentation in Silicon Errors in Logic – System Effects (SELSE), 2023.

[PP9] F. F. dos Santos, A. Kritikakou (*), and O. Sentieys, "Experimental evaluation of neutron-induced errors on a multicore RISC-V platform", Presentation in Silicon Errors in Logic – System Effects (SELSE), 2023.

2022

[PP8] F. F. dos Santos, P. Rech, A. Kritikakou (*), and O. Sentieys, "Evaluating the Impact of Mixed-Precision on Fault Propagation for Deep Neural Networks on GPUs", Presentation in IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Paphos, Cyprus, 2022.

[PP7] Qualis: B2 Core: B — M. Cui, A. Kritikakou (*), L. Mo, and E. Casseau, "Near-optimal Energy-Efficient Partial-Duplication Mapping of Real-Time Parallel Applications ", Presentation (2.0 publication model) in Int. Conf. Reliable Software Technologies (AEiC 2022), 2022, Ghent, Belgium

[PP6] F. F. dos Santos, A. Kritikakou (*), O. Sentieys, and P. Rech, "Characterizing Deep Neural Networks Neutrons-Induced Error Model", Presentation in IEEE Nuclear and Space Radiation Effects Conference (NSREC), Provo, Utah, 2022.

[PP5] R. Mercier, C. Killian, A. Kritikakou (*), Y. Helen and D. Chillet, "Tolerating Errors in NoC: A Lightweight Region-Based Fault-Mitigation Method", Presentation in Silicon Errors in Logic – System Effects (SELSE), 2022.

[PP4] F. F. dos Santos, A. Kritikakou (*), and O. Sentieys, "Experimental evaluation of neutron-induced errors on a RISC-V processor", Poster in RISC-V meeting, Paris, France, 2022.

2018

[PP3] Qualis: A2 Core: B — L. Mo, A. Kritikakou (*) and O. Sentieys, "Energy-Quality-Time Optimized Task Mapping for DVFS-enabled Real-Time Multicore", Presentation (2.0 publication model) in Embedded System Week: Int'l Conference on Hardware/Software Codesign and System Synthesis (ESWEEK: CODES+ISSS), 30 September - 5 October, Torino, Italy

2015

[PP2] Qualis: B2 Core: B — A.Kritikakou (+), F. Catthoor, V. Kelefouras and C. Goutis, "A Scalable & Near-optimal Representation for Storage Size Management", Presentation (2.0 publication model) in High Performance and Emdedded Architecture and Compilation (HIPEAC), 19-21 January 2015, Amsterdam, The Netherlands

2014

[PP1] Qualis: A1 Core: B — A. Kritikakou (+), F. Catthoor and C. Goutis, "Scalable & Near-optimal methodologies for memory management & processing of embedded systems", Poster in PhD Forum in Design, Automation & Test in Europe (DATE), 24-28 March 2014, Dresden, Germany

National conferences and symposium

2024

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