UNIVERSITÉ DE RENNES 1

Direction de la Recherche et de l'Innovation

Appel à projets - Année 2023

Contrats doctoraux «Ordinaires»

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Sujet

Titre : Automatic synthesis of secure & predictable processors for the Internet of Thing

Mots clés : Architecture des processeurs, Outils de CAO électronique,

Cotutelle internationale (oui/non) : non **Si oui, préciser l'établissement et le pays de rattachement** :

Descriptif (15-30 lignes) :
Contexte socioéconomique et scientifique ; Les hypothèses et questions posées ; Les grandes étapes de la thèse et démarche ; Approches méthodologiques et techniques envisagées

The vast majority of automotive and IoT platforms rely on low-power Micro-Controller Units, whose micro-architecture and instructions sets are highly customized. These customized processors are designed by hand using Hardware Description Languages. Designing a processor pipeline at this level of abstraction is very tedious, and extremely time consuming.

The ability to automatically infer a micro-architecture (or family of micro architecture) from a more abstract representation (e.g. a behavioral model of the processor ISA in C/C++) can be an answer to these issues, as it could streamline the design process while enabling early design space exploration. Unfortunately, current commercial High Level Synthesis flows, which translate C/C++ to hardware designs, are unable to efficiently deal with such inputs, because they lack the ability to take advantage of speculation. Recent research results have however shown that this limitation could be lifted, and that it was possible to automatically generate processor pipelines whose performance and area cost were comparable to manual designs, as demonstrated by the SpecHLS flow developed at IRISA.

New design issues are however emerging: in addition to performance and energy constraints, IoT hardware platforms must now also integrate security and predictability guarantees. Such guarantees are very challenging to enforce, as they involve a deep understanding of the underlying micro-architecture along with often subtle (and ad-hoc) changes to the HDL design. They can therefore only be implemented by domain experts, and only at the price of significant additional design efforts. Such non-functional guarantees also often adversely impact performance and hardware cost. As a consequence, choosing the best design involves a trade-off between conflicting requirements, and design time constraints often force designers to opt for sub-optimal solutions.

The goal of the thesis is to study and propose novel techniques for micro-architectural synthesis, in which non-functional properties are supported through domain specific analysis (for predictability) and transformations (for security). Because of its open license and growing popularity, the project will focus on the open-source RISC-V ISA.

➢ **Ce document est à renvoyer par la direction de l'unité de Recherche aux animateurs du Pole Recherche et à l'école Doctorale pour le 6 février 2023 au plus tard**