Personal information

First name / Surname : **Emmanuel Casseau**

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Nationality: French

Gender: Male



Current position & research interests

09/2006 - present: Professor

Department of Electronics, ENSSAT Engineering Graduate School, University of Rennes1, France. www.enssat.fr/en_US/home

IRISA laboratory/ INRIA, CAIRN team www.irisa.fr/en team.inria.fr/cairn

I'm currently the Head of the Department of Electronic Engineering (namely Department of "Digital Systems Engineering"), ENSSAT Engineering Graduate School, Lannion, France. http://www.enssat.fr/en_US/formations/formation-ingenieur-systemes-numeriques

Research keywords: embedded system design, high-level synthesis, mapping/scheduling techniques, fault-tolerant techniques and design, reconfigurable architectures and FPGA-based accelerators.

My research interests are in the broader area of computer architectures, where I investigate the design of high-performance and cost-effective embedded systems and reconfigurable-based architecture design. Within this context, I have performed research in high-level synthesis, mapping/scheduling techniques, custom and application-specific hardware architectures targeting multimedia and signal processing applications, reconfigurable architectures and FPGA-based accelerators. More recently, I focused on reliable architectures and fault-tolerant scheduling onto embedded multicore platforms.

Education

Research Habilitation: 12/2002, University of Bretagne Sud, Lorient, France, Design of architectures dedicated to dataflow applications and real time systems.

PhD: 06/1994 : University of Bretagne Occidentale, Brest, France, Systolic array based processor design for solving partial differential equations with finite element method.

M.Sc.: 07/1990, University of Bretagne Occidentale, Brest, France. Department of Electronics.

B.S.: 06/1988, University of Bretagne Occidentale, Brest, France. Department of Electrical Engineering.

Other working experience

08/2016 – 07/2017: Academic researching visitor in the Parallel and Reconfigurable Computing Group, Department of Electrical and Computer Engineering, University of Auckland, New Zealand.

09/1996 – 08/2006: Associate Professor, Department of Electronics, University of Bretagne Sud, Lorient, France.

10/1994 – 08/1996: Research Engineer in the French National Telecom Engineering Graduate School, ENST Bretagne, Brest, France.

Teaching experience

I have taught many courses in electronics and computer architecture, both at undergraduate and graduate levels, in the Department of Electronics of ENSSAT Engineering Graduate School and in the Department of Electronics of the University of Bretagne Sud. I also taught “Field-programmable gate arrays“ and "Processor architectures” it the University of Science and Technology of Hanoi, Vietnam.

Undergraduate courses:

- Analog electronics
- Digital electronics
- Processor architectures
- Real time design methodology
- Signal processing

Graduate courses:

- Digital communications
- Field-programmable gate arrays
- High-level synthesis
- Introduction to verification
- SoC design

Ph.D. graduates

PhD candidates: H.V.L. Nguyen (01/2020-present), M. Cui (09/2018-present),

PhD graduates: P. Dobias (2020), M.T. Tran (2018), J. Metairie (2016), H. Yviquel (2013), T. Chabrier (2013),C. Xiao (2012), S. Khan (2010), C. Andriamisaina (2008), F. Abbes (2007), S. Huet (2006),F. Sayadi (2006), B. Le Gal (2005), G. Savaton (2002), C. Jégo (2000).

Recent publications

Journals :

C. Xiao, S. Wang, W. Liu, X. Wang, E. Casseau, "An Optimal Algorithm for Enumerating Connected Convex Subgraphs in Acyclic Digraphs", *IEEE Transactions on Circuits and Systems II: : Express Briefs*, Volume: 68, Issue: 1, pp. 261 – 265, Jan. 2021.

C. Xiao, S. Wang, W. Liu, E. Casseau, "Parallel Custom Instruction Identification for Extensible Processors", *Journal of Systems Architecture*, Elsevier, Volume 76, pp 149-159, May 2017.

S. Wang, C. Xiao, W. Liu, E. Casseau, “A comparison of heuristic algorithms for custom instruction selection”, *Microprocessors and Microsystems : Embedded Hardware Design (MICPRO)*, Elsevier, Volume 45, Part A, pp 176-186, 2016.

H. Yviquel, A. Sanchez, P. Jääskeläinen, J. Takala, M. Raulet, E. Casseau, “Embedded multi-core systems dedicated to dynamic dataflow programs”, *Journal of Signal Processing Systems*, Springer, Volume 80, Issue 1, pp 121-136, 2015.

S. Khan, E. Casseau, D. Menard, “High performance Discrete Cosine Transform (DCT) operator using multimedia oriented subword parallelism (SWP)”, *Advances in Computer Engineering*, Hindawi, vol. 2015, 2015.

Conferences :

M. Cui, A. Critikakou, L. Mo, E. Casseau, “Fault-Tolerant Mapping of Real-Time Parallel Applications Under Multiple DVFS Schemes”, 27th IEEE Real-time and Embedded Technology and Applications Symposium, RTAS 2021, Samos Island, Greece, May 18-21, 2021

V. L. Nguyen Huu, J. Lallet, E. Casseau, L. d’Orazio, “MASCARA (ModulAr Semantic CAching fRAmework) towards FPGA acceleration for IoT Security monitoring”, International Workshop on Very Large Internet of Things (*VLIoT 2020*), Tokyo, Japan, September 4.

P. Dobias, E. Casseau, and O. Sinnen, "Evaluation of Fault Tolerant Online Scheduling Algorithms for CubeSats”, 23rd EUROMICRO Conference on Digital System Design, Portoroz, Slovenia, August 26-28, 2020.

M. Cui, A. Critikakou, L. Mo, E. Casseau, “Energy-aware Partial-Duplication Task Mapping under Real-Time and Reliability Constraints”, 20th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, SAMOS XX, Samos Island, Greece, July 5-9, 2020

P. Dobias, E. Casseau, and O. Sinnen, "Fault-Tolerant Online Scheduling Algorithms for CubeSats”, *11th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architecture, 9th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM’20)*, Bologna, Italy, January 21, 2020.

Rafail Psiakis, Angeliki Kritikakou, Olivier Sentieys, E. Casseau, "Run-time Coarse-Grained Hardware Mitigation for Multiple Faults on VLIW Processors”, *Conference on Design and Architectures for Signal and Image Processing (DASIP)*, Montreal, Canada, pp.1-6, October 16-18, 2019.

P. Dobias, E. Casseau, and O. Sinnen, “Restricted Scheduling Windows for Dynamic Fault-Tolerant Primary/Backup Approach-Based Scheduling on Embedded Systems”, *SCOPES '18: 21th International Workshop on Software and Compilers for Embedded Systems*, Sankt Goar, Germany, May 28-30, 2018.

I. Wali, E. Casseau, A. Tisserand, “An Efficient Framework for Design and Assessment of Arithmetic Operators with Reduced-Precision Redundancy”, *Conference on Design and Architectures for Signal and Image Processing (DASIP)*, pp.1-6, 2017.

M.-T. Tran, M. Gautier, E. Casseau, “On the FPGA-based implementation of a flexible waveform from a high-level description: Application to LTE FFT case study”. *EAI International Conference on Cognitive Radio Oriented Wireless Networks (Crowncom 2016)*, pp. 545-557, 2016.

J. Métairie, A. Tisserand, E. Casseau, “Small Multiplication-Inversion Unit for Normal Basis Representation in GF(2^m)”, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 440-445, 2015.