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ESL: Panacea or Hype?

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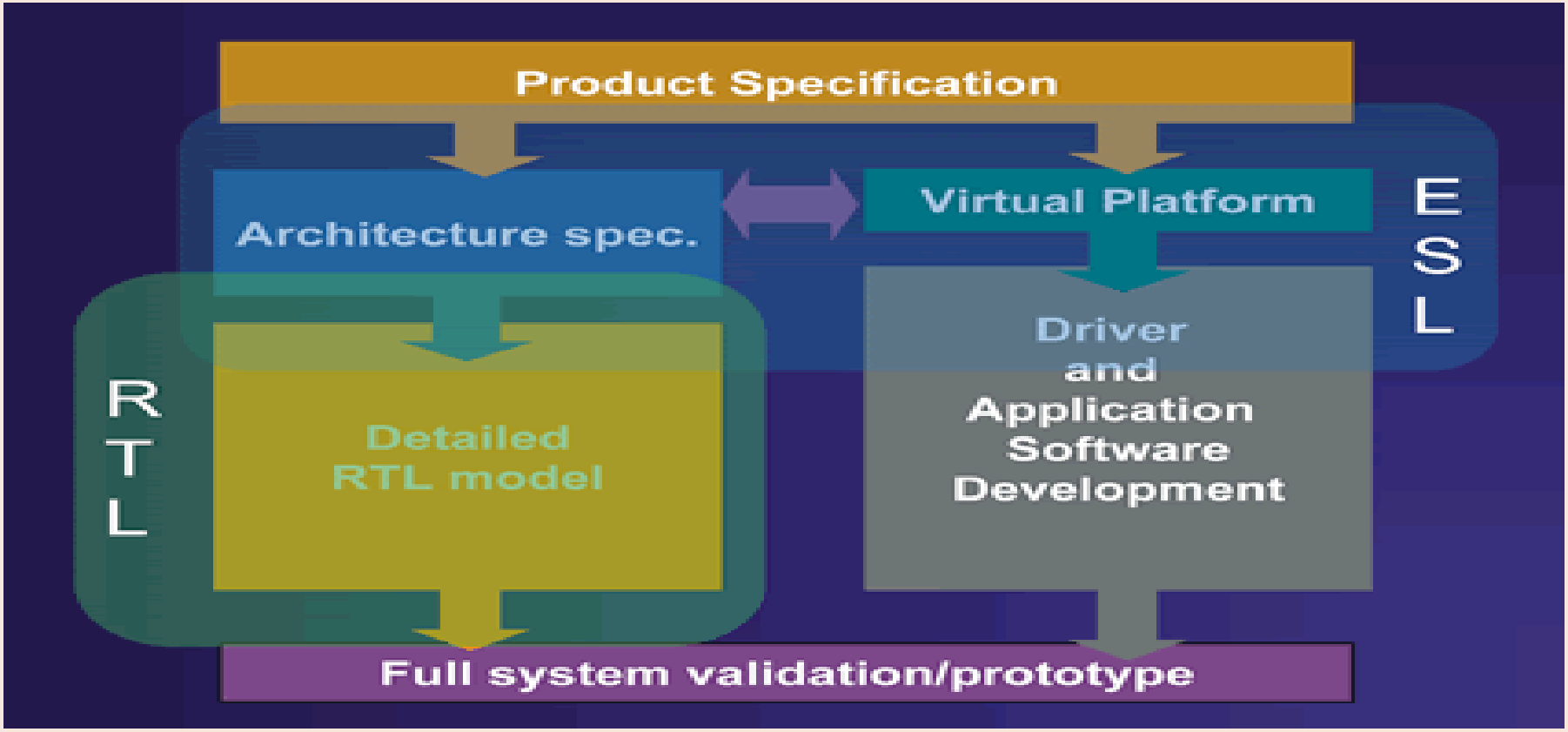
FERMAT @Virginia Tech, and
the "Chip Design" Magazine

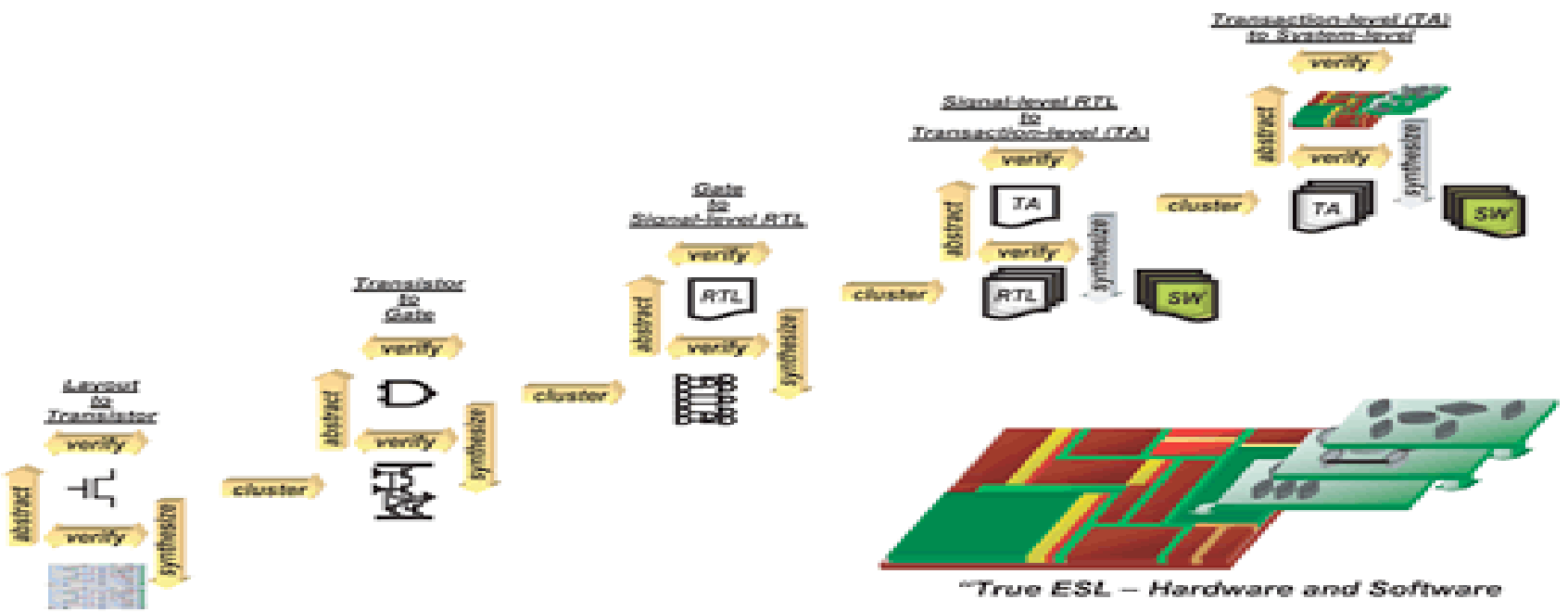
Outline

- Pictures speak louder than words
  - What is ESL?
  - Abstraction Trends
  - Verification Trends
  - EDA Industry Trends
- What are we doing?
  - Heterogeneity and MoCs
  - Behavioral Hierarchy
  - Meta Modeling Support
  - Service Oriented Validation Framework

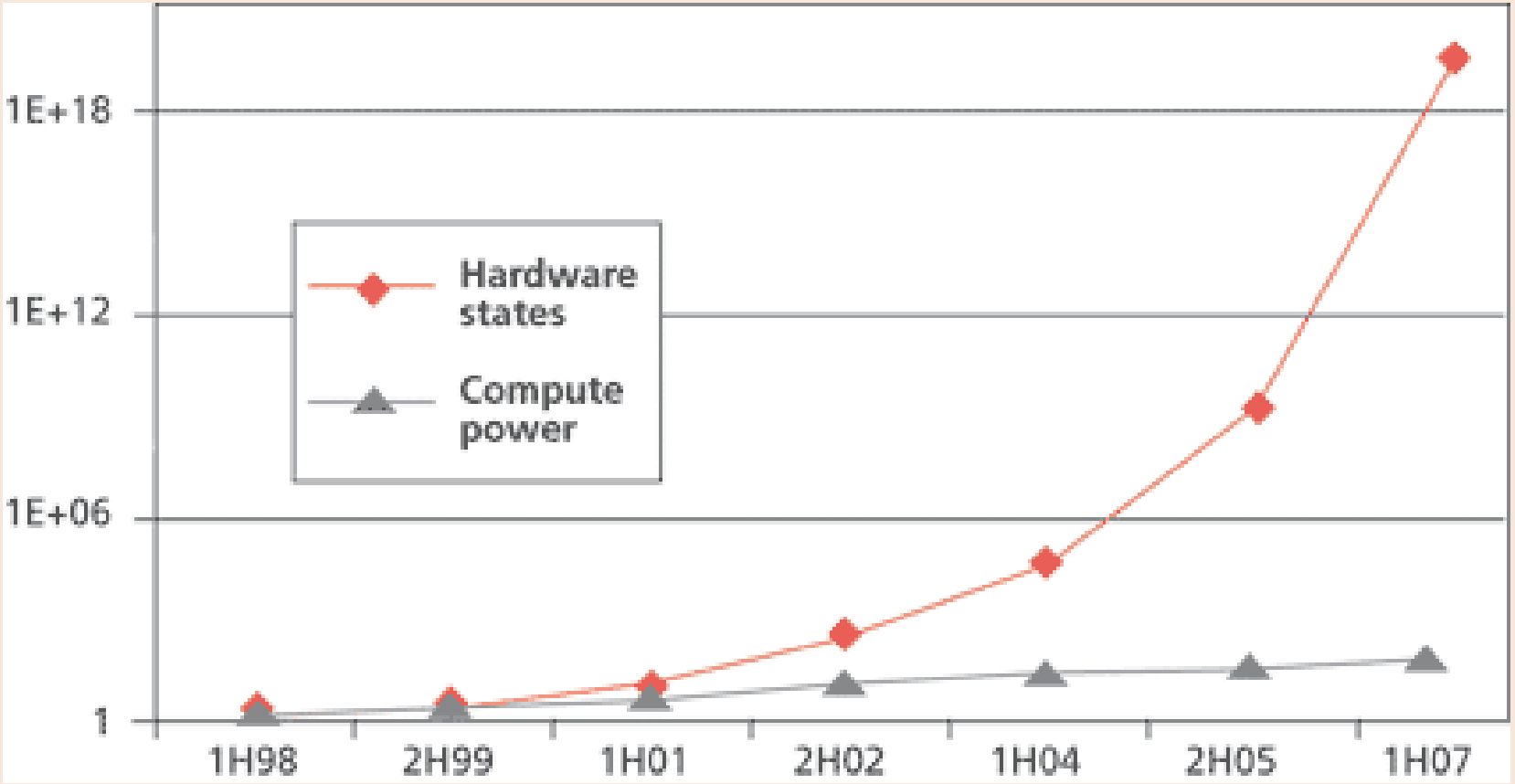
Electronic System Level?



Abstraction Trends



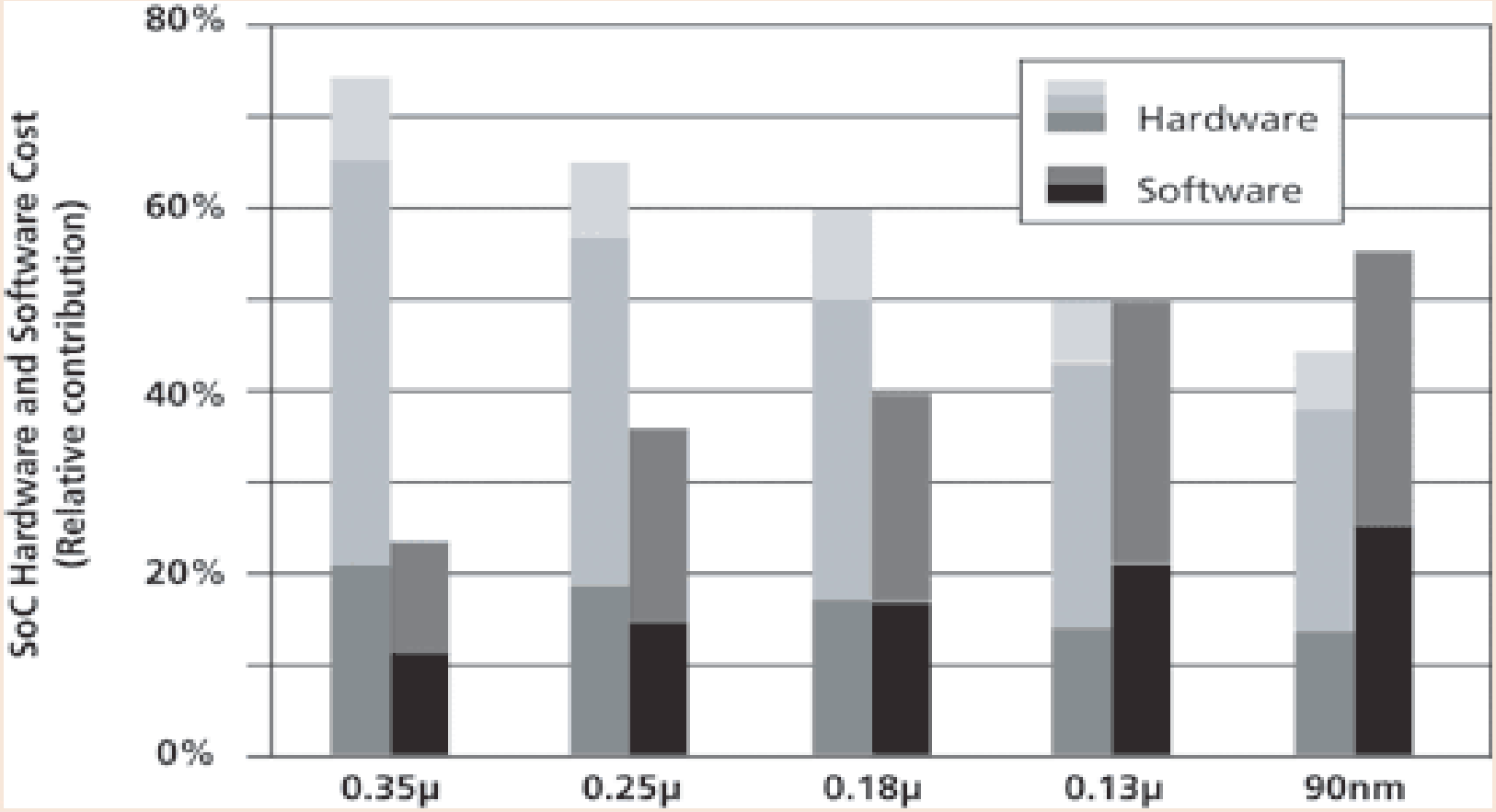
Hardware Resources and Computer Power



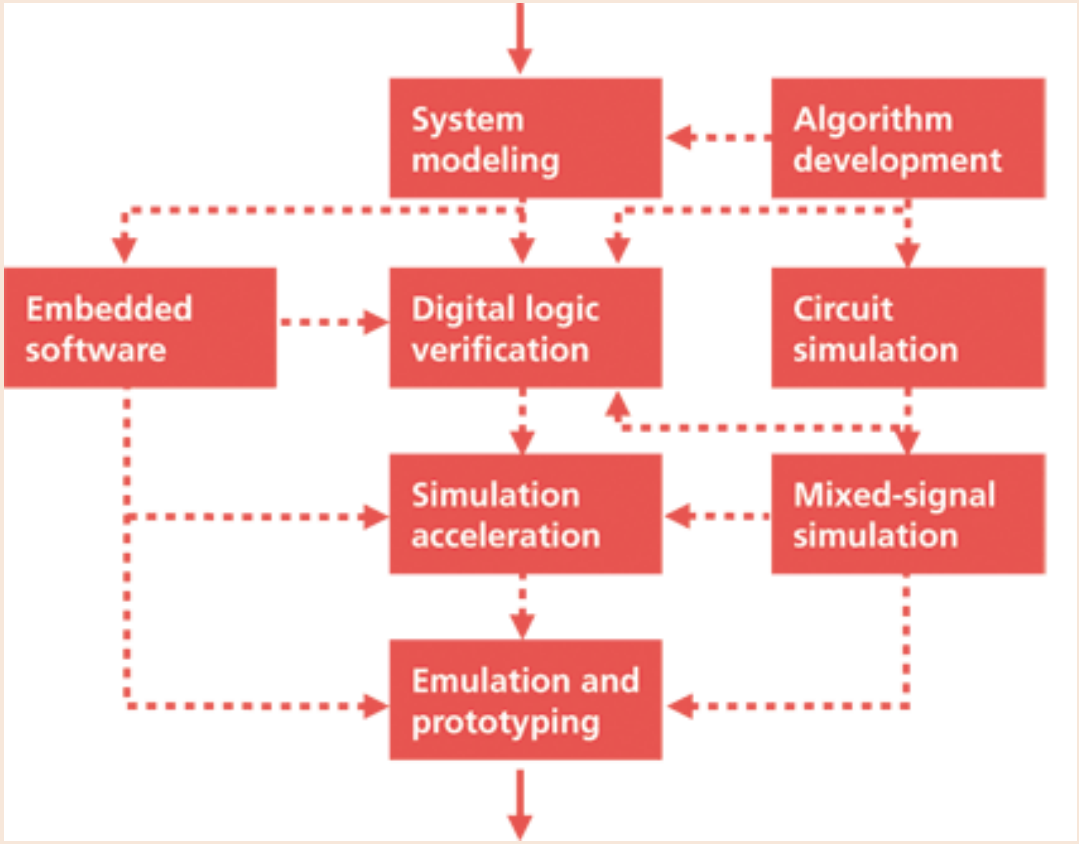
A Tale of Two ESLs?

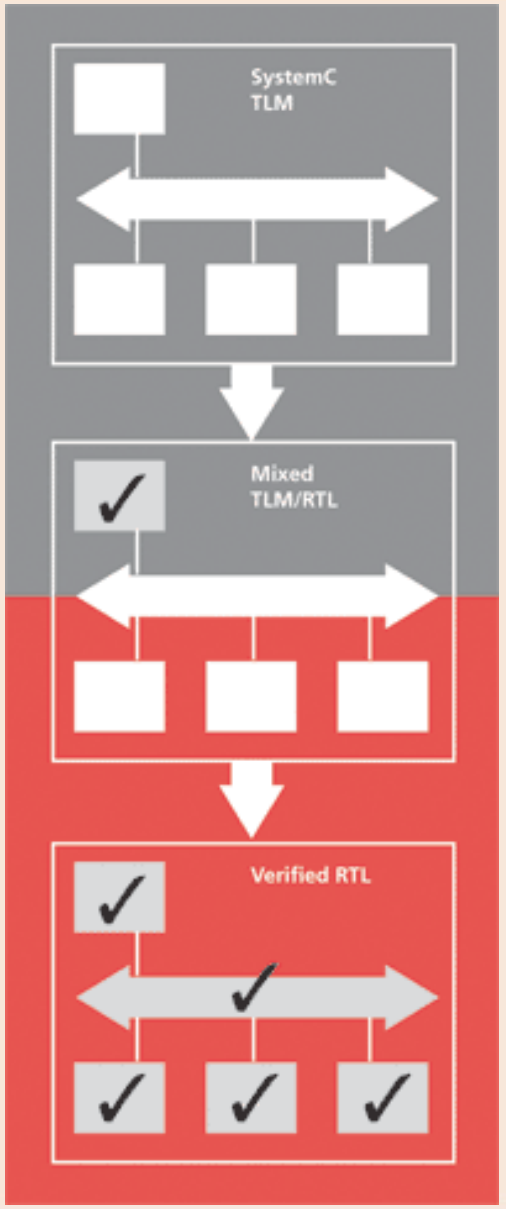
	SystemC	SystemVerilog
Core abstration level	Events and messages	Logic states and transitions
Architectural design	System-level hardware view and SW programmer's view	HW implementation view; DPI link to C/C++/SystemC
Architectural verification and HW/SW co-verification	Cycle accurate TLM@ >10,000 cps	Timing accurate RTL @ 1-10 cps; TLM capability; C-like extensions for algorithmic descriptions
RTL-to-gates design	No gate-level modeling	Logic synthesis
RTL-to-gates verification	TLM/RTL co-stimulation	Implementation testbench, including ABV and functional coverage

HW/SW Cost Breakdown Trends

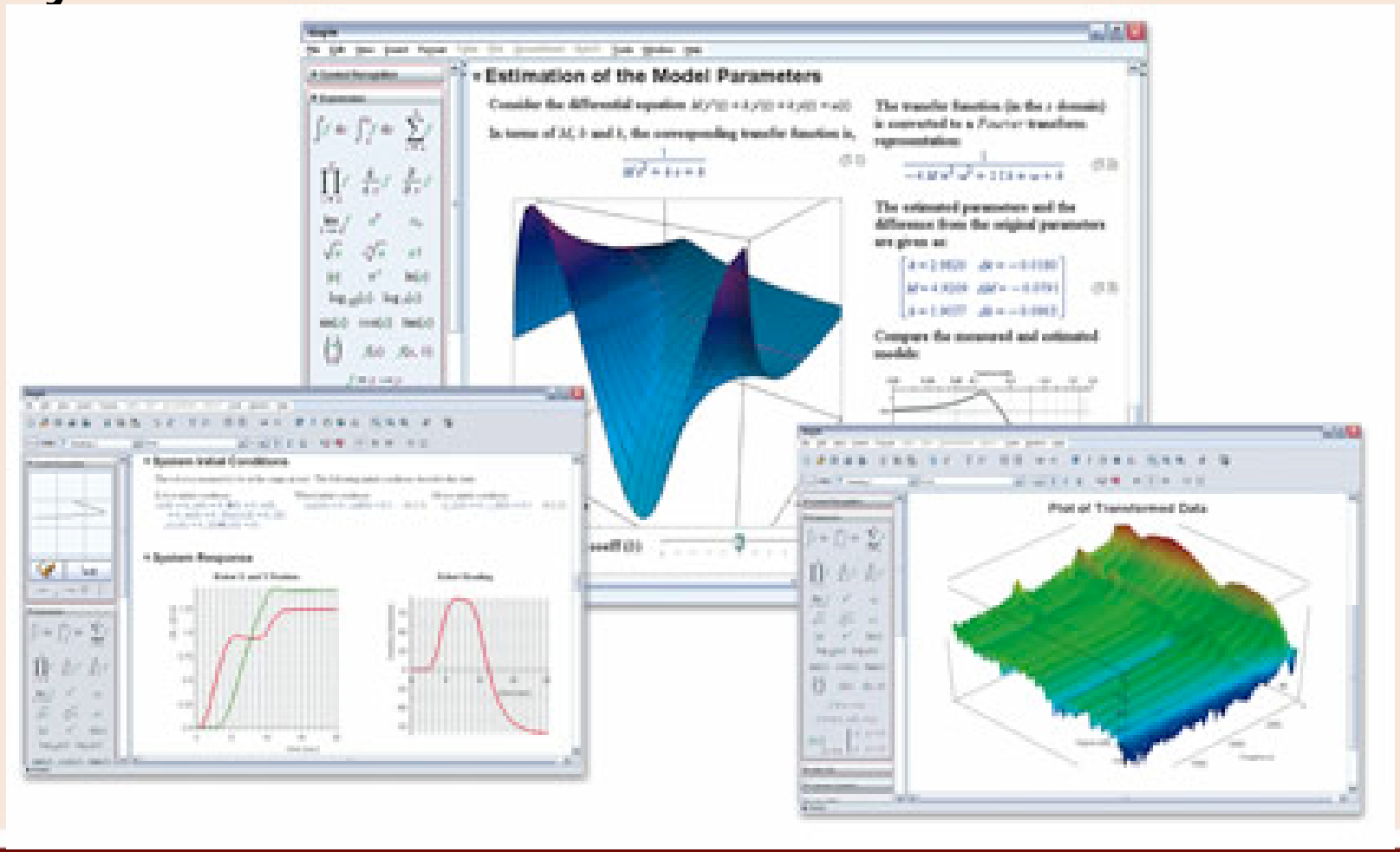


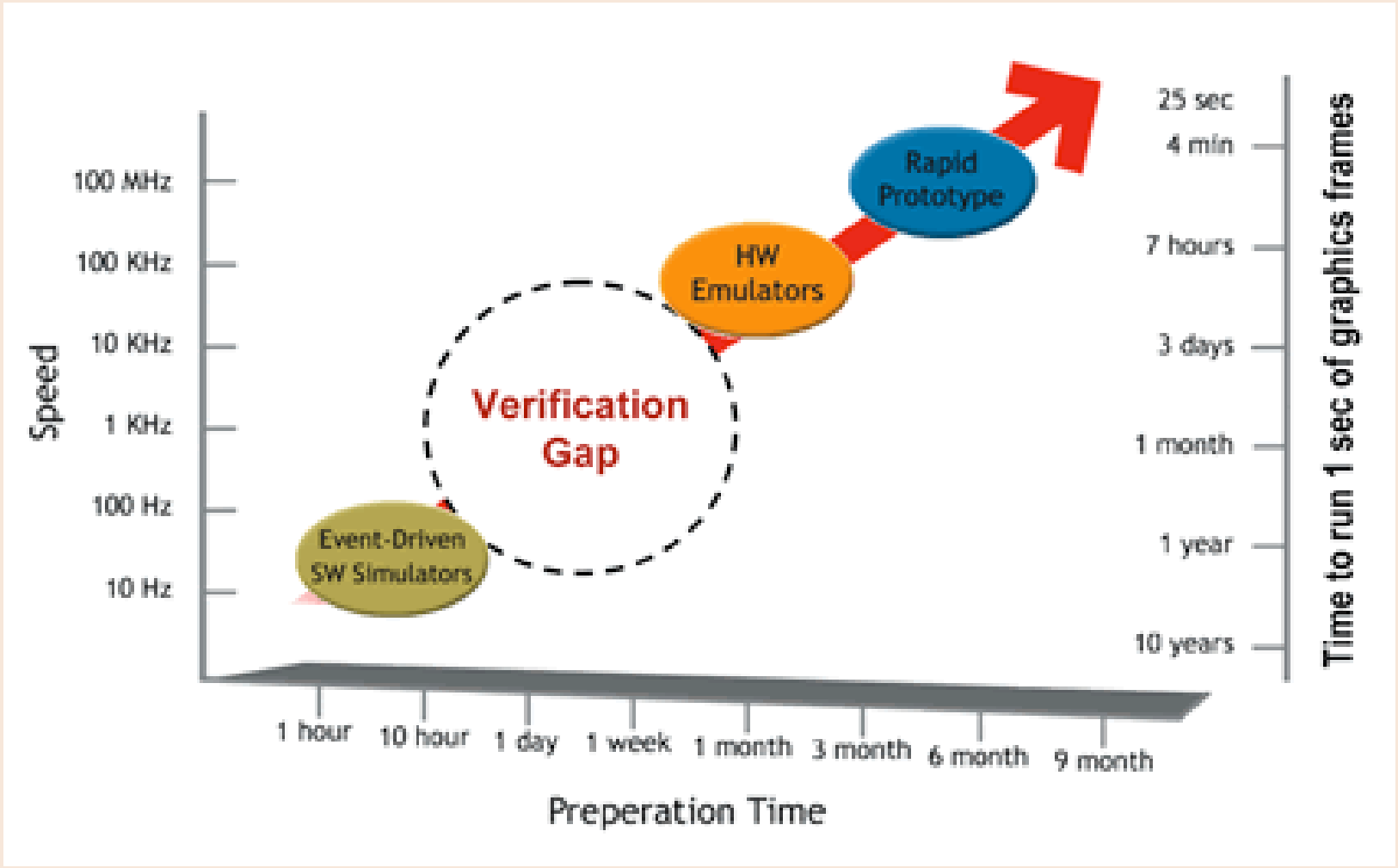
Verification Trends



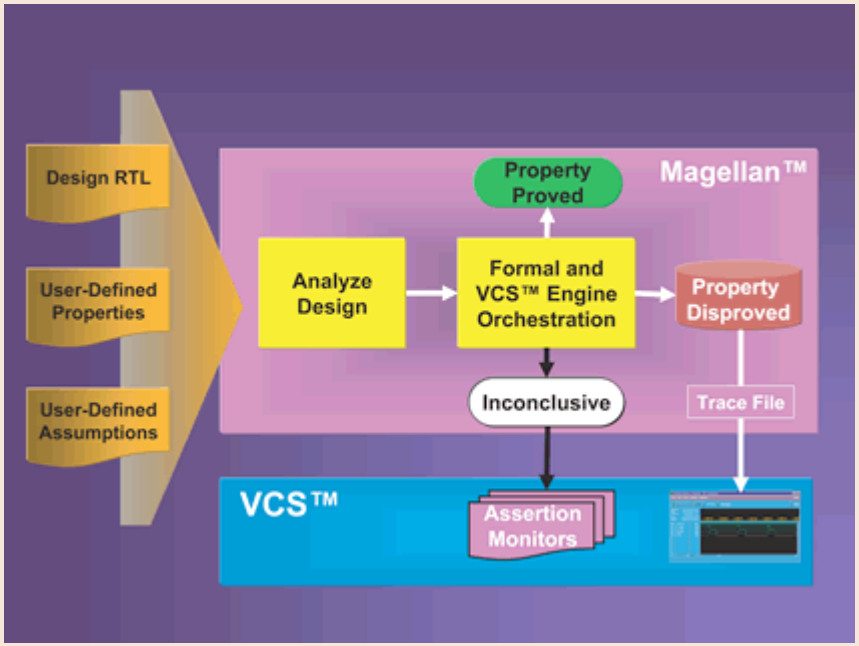


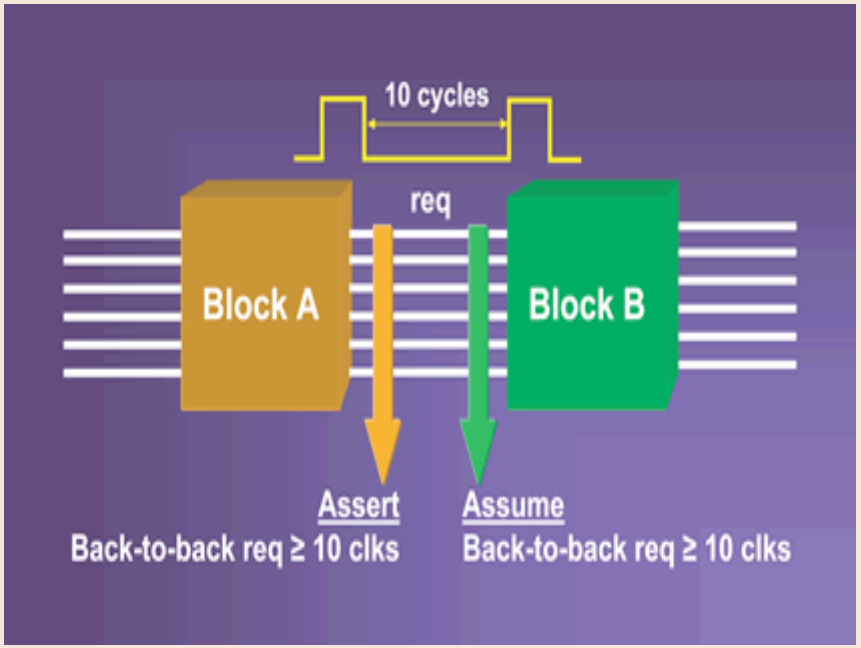
Hybrid and AMS




Speed
100 MHz
100 KHz
10 KHz
1 KHz
100 Hz
10 Hz
Event-Driven SW Simulators
Verification Gap
HW Emulators
Rapid Prototype
25 sec
4 min
7 hours
3 days
1 month
1 year
10 years
Time to run 1 sec of graphics frames
1 hour
10 hour
1 day
1 week
1 month
3 month
6 month
9 month
Preperation Time

Verification Trends





ESL Industry Space

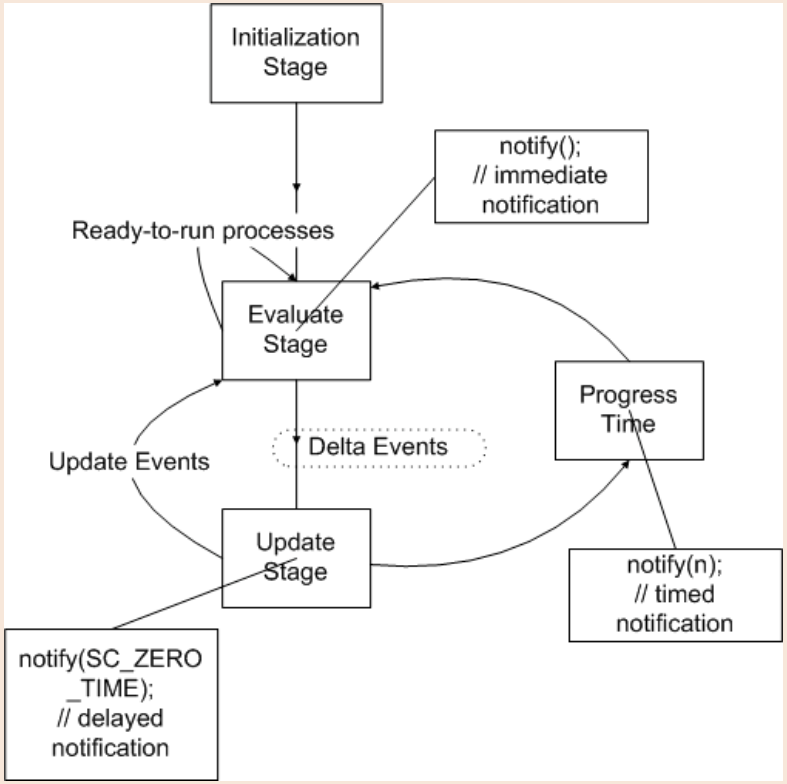
Company	Location	Design Style	Design Language	Capabilities	Url
ACE Associated Compiler Experts bv	Amsterdam, The Netherlands	Embedded	C/C++	Compiler generators & testing tools for compilers	www.ace.nl
Aldec, Inc.	Henderson, NV	SoC	C/C++, Handel-C, Verilog, VHDL	ASIC & high-density FPGA verification environment	www.aldec.com
Alternative System Concepts, Inc.	Windham, NH	Embedded	XML, Verilog, VHDL	Behavioral synthesis software tool to reduce power consumption	www.asicnc.com
Altera Corp.	San Jose, CA	Embedded	C, MATLAB, proprietary	Automates adding, parameterizing, & linking embedded processors, co-processors, peripherals, memories, user-defined logic for system-on-a-programmable-chip	www.altera.com
Ansoft Corp.	Pittsburgh, PA	Component	VHDL-AMS	Mixed-technology designs prevalent in automotive industry	www.ansoft.com
ARM Ltd (acquired AXYS Design Automation)	Cambridge, UK	SoC	C/C++, SystemC, LISA	Simulation, debugging, analysis, verification. Cycle and functionally accurate virtual prototyping. Transaction-based abstraction level	www.arm.com
BlueSpec	Waltham, MA	Behavioral	SystemVerilog	SystemVerilog-based behavioral synthesis	www.bluespec.com
Cadence Design Systems, Inc.	San Jose, CA	Behavioral Co-Verification	C/C++, SystemC, Verilog, VHDL	Transaction-level model development & verification, algorithm development, hardware-software verification	www.cadence.com
Carbon Design Systems	Waltham, MA	Behavioral	C, Verilog, VHDL	Virtual hardware models from Verilog and/or VHDL	www.carbondesignsystems.com
CARDtools Systems	San Jose, CA	SoC, embedded	C/C++	Modeling hardware, software, & systems at different levels of abstraction	www.cardtools.com
Catalytic Inc.	Palo Alto,	SoC, embedded	MATLAB from	Signal processing algorithm	www.catalytic-inc.com

Our Work at FERMAT and ESPRESSO

- Introduce Heterogeneity in SystemC with Models of Computation (MoC) extensions
- Raise the Modeling Fidelity
- Step towards Behavioral Hierarchy with Heterogeneity
- EWD: Meta-Modeling Frameworks
- CARH: Service Oriented Validation Framework

SystemC's Discrete-Event Kernel

- Evaluate-Update Paradigm
- Dynamic scheduling incurs unnecessary delta cycles
- Statically schedulable MoCs should avoid dynamic scheduling



An Example MoC Extension: Synchronous Data Flow in SystemC

- SDF models are:
  - Amenable to static scheduling
  - Require blocks to have predefined production and consumption rates
  - Construct repetition vector
  - Construct firing order
  - Executable schedule achieved with valid repetition vector and firing order

An Example MoC Extension: Synchronous Data Flow in SystemC

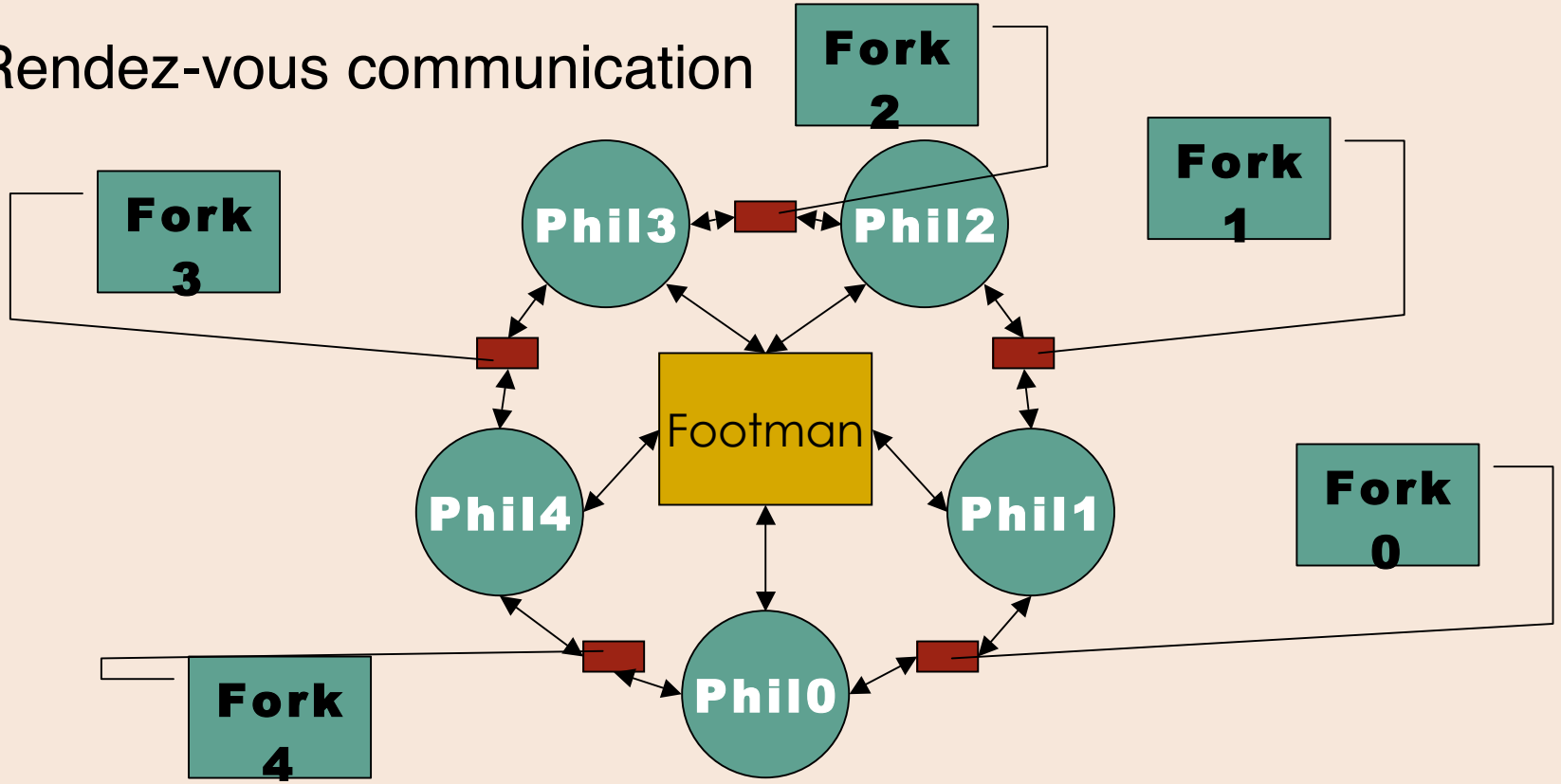
```
SC_MODULE( toplevel )
{
        sc_in_clk CLK;
        SC_THREAD( topentry )    {
          sensitive << CLK.pos();
        };
        SC_CTOR ( toplevel ) {
          // Instantiate SDF blocks and connect
          // the ports
        }
        void topentry() {
          sdf_trigger();
        }
};
```

An Example MoC Extension: Synchronous Data Flow in SystemC

- During initialization all executable schedules are computed
- DE kernel continues executes without intervention until sdf_trigger() is invoked
- SDF kernel takes over and executes the SDF-specific blocks according to the computed schedule

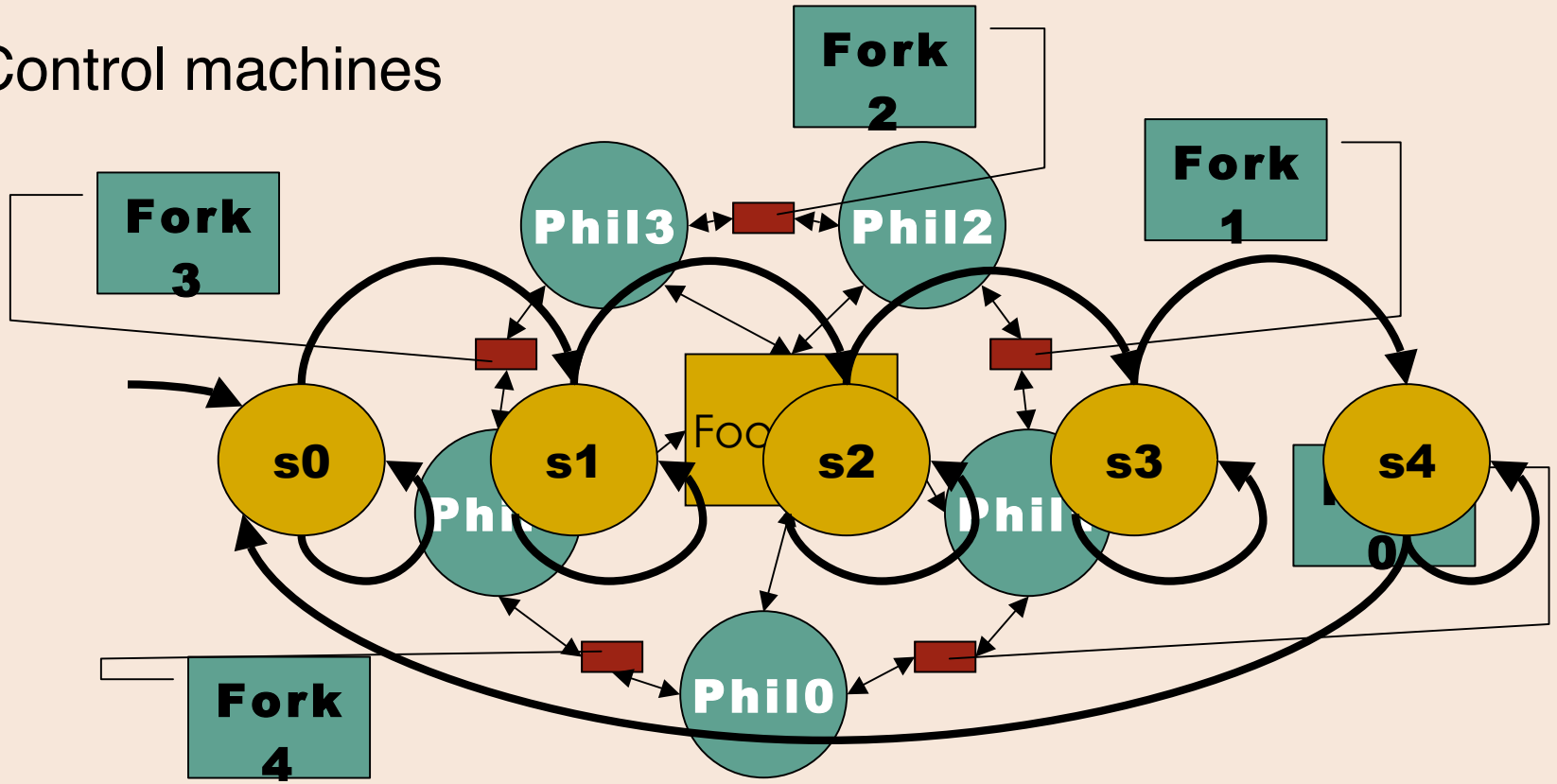
Heterogeneous Extensions Communicating Sequential Processes

- Rendez-vous communication

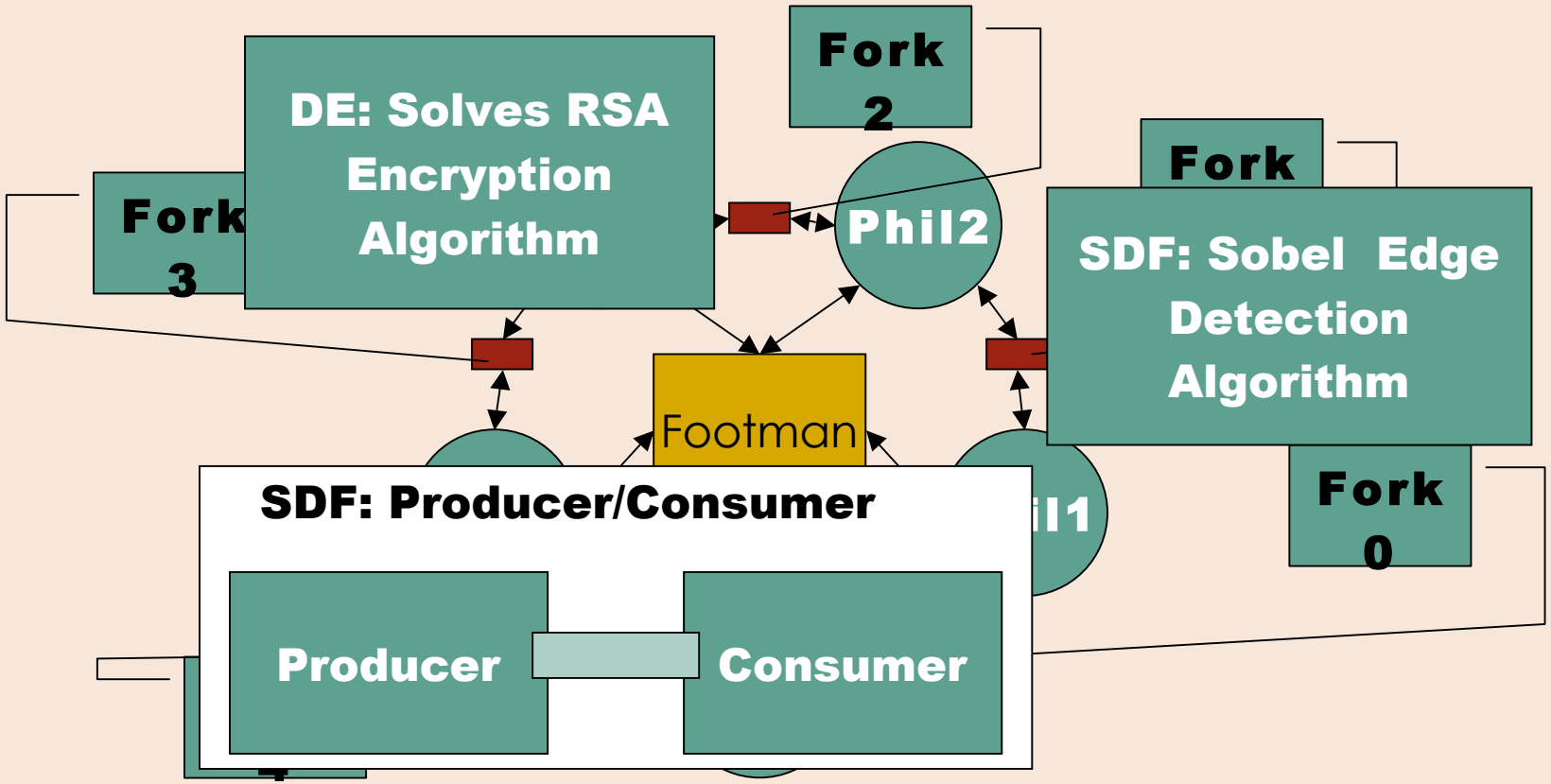


Heterogeneous Extensions Finite State Machine

- Control machines



Heterogeneous Extensions
DE, FSM, SDF & CSP

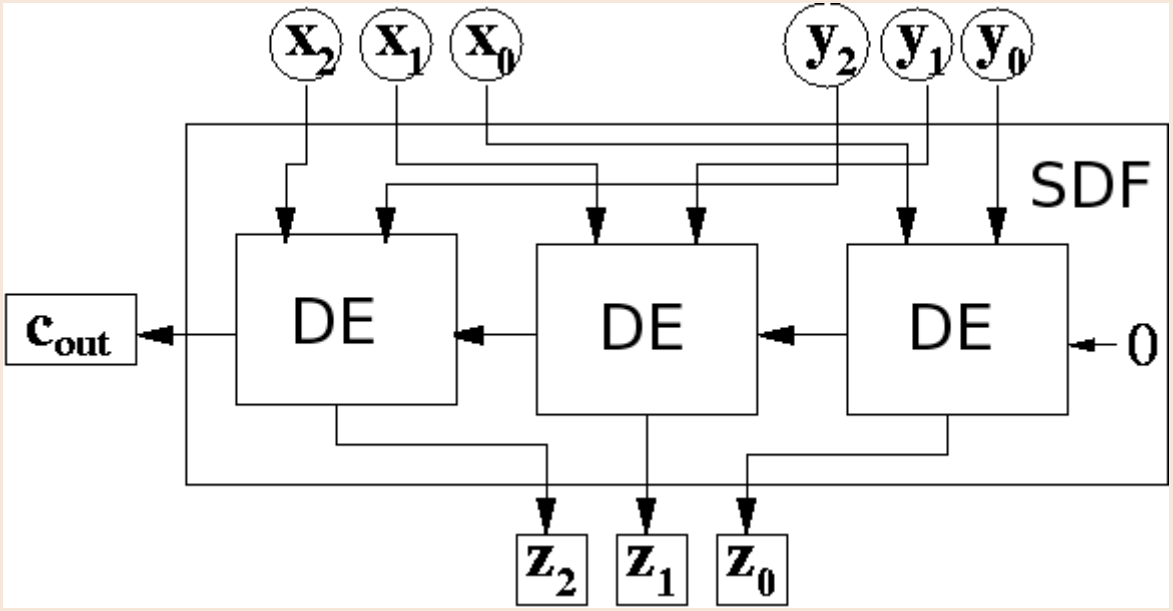


Simulation Efficiency
A brief look

- Pure SDF models ~ 65% gains
- Pure FSM models ~ 10% degradation
- Pure CSP models ~ 1% gains

Behavioral Hierarchy with Heterogeneity

- Decompose design into small behaviors
- Behaviors expressed by different MoCs

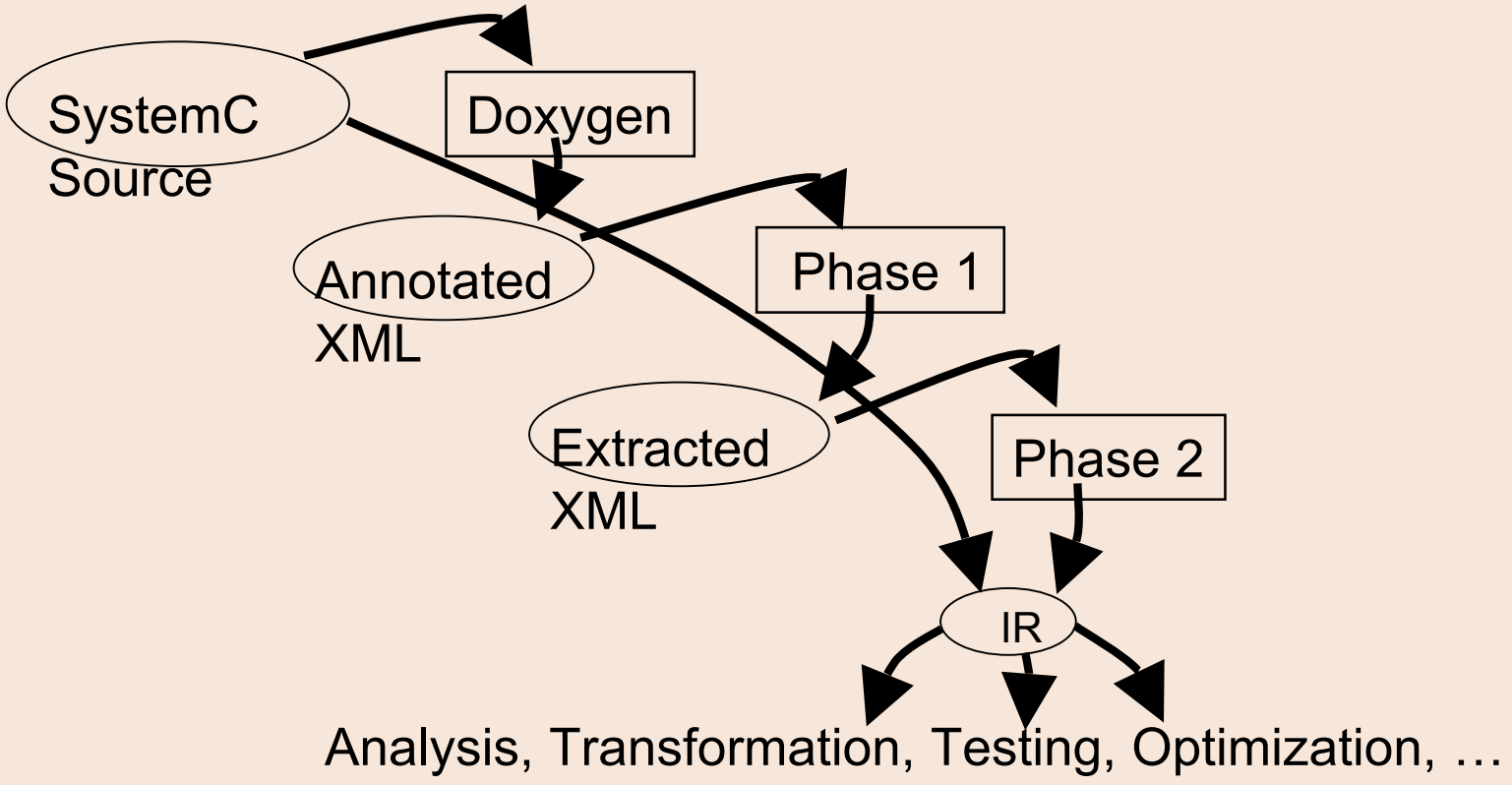


Behavioral Hierarchy with Heterogeneity

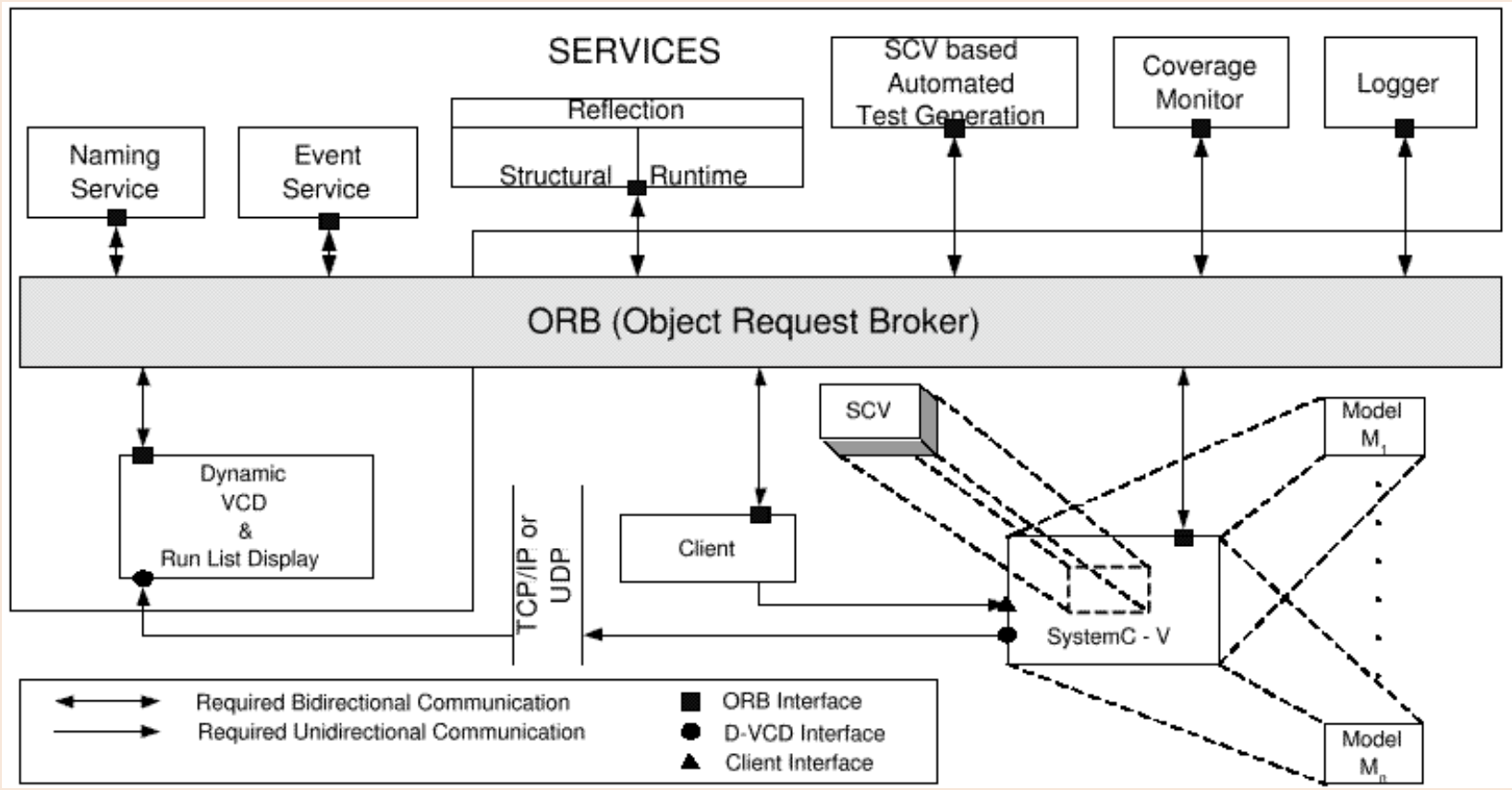
- Semantics define interactions within MoC and across MoCs
- Hierarchical composition preserves behavioral hierarchy

Why you want GreenSocs

- SystemCXML: http://systemcxml.sourceforge.net



What we do with SystemC?

- 

Reference

- Website for SystemC-H: http://fermat.ece.vt.edu/systemc-h/
- Book