Curriculum vitae
Thierry Jéron
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**Personal information**

- **Name:** Thierry Jéron
- **Date and place of birth:** June 7th, 1963, St Brieuc (France)
- **Citizenship:** French
- **Sex:** Male
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**Education**


- Ph. D. in Computer Science, University of Rennes 1, may 1991, “Contribution à la validation de protocoles : test d’infiniitude et vérification à la volée”.

- Master in Computer Science and Magister in Mathematical Modélisation and Computer Science Methods, 1988, University Rennes 1.

**Professional Career**

- **April 2001-Today:** Research Scientist and Scientific Leader, VerTeCS research team, Iriva/Inria Rennes.

- **January 1993-April 2001:** Research Scientist, Pampa research team, Iriva/Inria Rennes.


- **June 1991- November 1991:** Expert engineer, Pampa research team, Iriva/Inria Rennes

- **October 88 - May 91:** Ph. D. Student, supervised by Claude Jard ADP research team, Iriva/Inria Rennes.
Ph. D. supervision and jury

Supervision of Ph. D. students


Valery Tschaen (since 2001). “Modèles et techniques de la synthèse de tests et de la synthèse de contrôleur.” Relations between test generation and controller synthesis.

Camille Constant (since 2004) with V. Rusu. “Vérification et test symboliques pour les systèmes réactifs”. Combination of verification and symbolic test generation applied to voice services in the context of a France Telecom grant.

Tristan Le Gall (since 2004) with B. Jeannet. “Treillis abstrait pour le type de donnée "file d’attente" pour la vérification et la synthèse de contrôleurs”. Verification of communication protocols by abstrat interpretation.


Jeremy Dubreil (since 2006) “Formal methods for testing and supervision of security in networks”

Jury member of the dissertations of:


Manuel Aguilar: “Contribution à la validation de systèmes de processus communicants par files d’attente : analyse statique pour la réduction de files”, University of Grenoble, December 2003 (reviewer).


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Cyril Pachon: Une approche basée sur les modèles pour le test de robustesse, University Joseph Fourier, Verimag, Grenoble, (rap), Octobre 2005 (reviewer).

Gregory Lestienne: LRI Orsay, nov 2005

Franck Lebeau: Génération de tests à partir de statecharts fondée sur le calcul de comportements, University of Franche Comté, Besançon, 8 dec 2005 (reviewer).

Alban Gratien: Diagnostic décentralisé et en-ligne de systèmes à événements discrets reconfigurables, University of Rennes, 13 dec 2005.

Bram de Wachter: dSL, a Language and Environment for the Design of Distributed Industrial Controllers, Université Libre de Bruxelles (ULB), 2 and 16 December 2005.

Program committees

- Steering Committee of MOVEP 2006 (Bordeaux) and MOVEP 2004 (Bruxelles),
- Program Committee TACAS 2006 (Vienna, Tool Chair), and TACAS 2005 (Edinburgh),
- Program Committee TESTCOM 2006 (New-York), TESTCOM 2005 (Montréal), TESTCOM 2004 (Oxford),
- Program Committee FATES 2005 (Edinburgh), FATES 2004 (Linz), FATES 2003 (Montréal), co-chair of FATES 2002 (Brau), PC of FATES 2001 (Aalborg).
- Program Committee ROSATEA 2006 (ISSSTA workshop, Portland),
- Program Committee LFM 2000 (Williamsburg, Virginia)
- Financial Chair of ISSRE 2004 (St Malo).

Grants and contracts

NB: marked with * are those grants and contracts in which I was the scientific leader for Irisa or the main contributor.

Grants relative to TGV

DGA-Vélilog (95)*: grant for DGA (Direction Générale de l’Armement) with Vélilog, Cap Sesa, le CNET, Célar, Verimag and Irisa. Design and coding of the 1st version of TGV.

TestComposer (99)*: with Vélilog, le CNET, Verimag and Irisa. Design, coding and experiment of TestComposer in the ObjectGéode toolbox (Verilog-Telelogic).

Forma (96-99)*: contract funded by CNRS and Research Ministry. Action with CNET, Verimag, LSV (ENS Caen), LaBri (Bordeaux). First connection of TGV with ObjectGéode and experiment on the SSCOP protocol.


Van Gogh (99-2001)*: collaboration between Twente University and Irisa on test synthesis. Comparison of TGV and Torx on case studies.

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RNTL COTE (2001-2002): with Softeam, FT R & D, Gemplus, AQL, LSR Imag and Irisa on testing for UML components. Definition of a UML profile for testing (impact on OMG’s U2TP) and integration of TGV with Objecteering, Umlaut, Tobias and Casting.

European Project IST Agedis (2000-2004)*: IST European project with IBM Haifa (Israël) and IBM Hurley (G-B), Imbus (D), Intrasoft (Gr), FT R & D (Fr), University of Oxford (G-B), Vérimag and Irisa. Design and development of a toolbox for test synthesis and execution for UML distributed components. The test synthesis tool is an integration of Gotcha principles (IBM) in TGV.

Grants relative to symbolic testing and STG

Verdon (98-99)*: Inria action with Inria teams Vasy (Grenoble), Meije (Sophia), Pampa (Irisa) and LSR Imag. Treatment of data for verification and testing.

CPS/Schlumberger (2001)*: in the context of GIE Bull-Inria, then with a direct collaboration with CPS-Schlumberger, with the Vasy team. Symbolic test synthesis for smart-card applications. Design and coding of a first version of STG, experiments.

ARC Inria Modocop (2002-2004): Inria research action with Inria teams Lemme and Oasis (UR Sophia), Vasy (UR Rhône-Alpes), Vérimag, LIFC (Besançon), Lande and VerTeCS (Irisa). Verification and testing for OO concurrent languages (Java and JavaCard) Comparison of STG with BZ-TT (LIFC) on the CEPS (electronic purse) case study.

CRE France Telecom (2004-2006)*: external research contract (CRE) funded by France Télécom R&D Lannion on testing of voice services. FTR&D already uses TGV-Agedis and wishes to use symbolic techniques for a better treatment of data.

European Network Artist2 (2004-2006): Network of Excellence on embedded systems. Partners of the Verification and Testing cluster with Aalborg (Danemark), Twente (Hollande), Liège and Bruxelles (Belgique), Vérimag (Grenoble) and LSV (Cachan).

Grants relative to security


Grants relative to automotive

European Project Esprit Modistarc (97-99): with Dassault Electronique, and several manufacturers and academics. Test generation from SDL specifications of automotive applications.

Other grants

Védam: during my Ph. D., participation to a contract with Véridal, France Télécom, Verimag and Irisa. Transfer of on-the-fly verification techniques in Védam (Verilog). Re-used in its successor ObjectGeode (Teelogic).

Alcatel: during my stay in Alcatel, test of embedded systems in trains for GEC Alsthom, and European RACE project Spex (work on model-checking).

Working group Test-Objets: (99-2000) work group piloted by LAAS, LRI and Irisa on OO testing.

AS Testic*: (2002) research action with LAAS, LRI, LaBri, Verimag and Irisa on robustness testing. ACI Security V3F: (2003-2005) with I3S (Nice), LIFC (Besançon), and CEA. Verification and testing for programmes with floating point numbers.

Collaboration Urbana-Verimag-Inria: (2005-2006) cooperation with Urbana Champaign and Verimag on runtime verification, monitoring, conformance testing and diagnosis.

Reviewing on projects proposals

- Open Technology Program of the Dutch Technology Foundation STW, 2005
- ARA SSIA and ACI SI, 2005
- RNTL, 2003, 2005
- Capes-Cofecub Franco-Bresilian cooperation

Responsabilities

- Scientific leader of Inria project team VerTeCS since 2001.
- Member of the Specialists Commissions of ENS Cachan (1998-2003), and IFSIC-University Rennes 1 (2002-2004).
- Jury member for Inria research positions in Rennes (2003-2004)
- Jury member for secretary positions in Rennes (2002).
- Elected at the Lab Council from 88 to 91 (as Ph. D. student representative) and from 2000 to 2004 (as scientist representative).
- Elected at Inria Scientific Council (substitute) from 1997 to 2000.

Teaching

EnstB Rennes (3rd year): since 94, protocol validation, model-checking and testing.

EnstB Brest (2nd year): from 2001 to 2004, testing.

3xI Brest: from 95 to 96, protocol validation.

DIIC 3, University of Rennes: from 94 to 2003, protocol validation, model-checking and testing.

Master in Computer Science, University of Rennes:
- From 2000 to 2002, computability and complexity.
- From 2002 to 2006, testing (broadcasted to Lannion, Brest and Vannes from 2002 to 2005).
Summary of research activities

My research activity lies in the context of the validation of reactive systems. The main objective is to improve their reliability by using formal methods, i.e., founded on mathematical models and theories. More precisely, I have been interested in verification of properties on models (model-checking, control), and “dynamic” validation of real systems with respect to their models (e.g. observation, testing, diagnosis). This research goes from theory to practice: definition of models, formalization of validation problems, conception of algorithms and development of tools, transfer in academia and industry, and teaching of validation techniques. The most successful achievement is the conception of test generation algorithms developed in the TGV tool. Very novative when started, TGV has been quickly internationally recognized. It is still up to date and motivates other research on testing. Hereafter, I summarize the most significant research activities.

Verification

Verification consists in checking that a model of a system satisfies some properties. In this context, I have been interested in asynchronous systems modelled as communicating automata, with potentially infinite state spaces, and for which most problems are undecidable.

**On-the-fly verification:** We have conceived a generic algorithm for on-the-fly verification, i.e. for verification during the construction of the state space of the model. This algorithm has been applied for model-checking linear temporal logic and for unboundedness testing for communicating automata [18, 6]. The algorithm has been transferred in the Veda (Verilog) and ObjectGéode (Verilog/Telelogic) tools, two well known tools for the validation of telecommunication protocols.

**Parallel verification:** I have conceived a parallel verification algorithm for communicating automata, and implemented it on parallel machines. It is interested to see that such algorithms are still up-to-date with grids.

**Verification of infinite state systems:** During my Ph. D., I have conceived and implemented a semi-decision procedure (decision procedure for a well defined sub-class) for the unboundedness of automata communicating through fifo channels [19, 7]. Later I supervised the Ph. D. of Y.-M. Quemener (93-96), during which we extended this procedure in an algorithm that extracts a graph grammar finitely representing the infinite state space [26] and allows model-checking of CTL [23]. I now co-supervise Tristan Legall’s Ph. D. On the same model, we propose a computation of an approximate reachability set based on abstract interpretation [57], and an extension for models with data.

**Graphical “verification”:** I conceived and developed the Viscope tool which allows to represent state graphs of concurrent processes in 3 dimensions [22, 50], with an explicit representation of concurrency and sequentiality.

**Control of discrete event systems:** Control consists in ensuring that a (finite) model satisfies its properties by forbidding some controllable actions. In the context of V. Tschäen’s Ph. D., we were interested in the relation between testing and controller synthesis. In [55, 41, 12] we showed how to ensure the conformance of an implementation with respect to its specification using control theory.

Dynamic validation

Since 95, most of my research concentrates on model-based conformance testing for non-deterministic reactive systems. In particular, we attack one of the most challenging problem in testing, which is automatic test generation from formal models of systems. My habilitation document [2] focuses on these works for enumerative models and on-the-fly techniques, and on models with data with symbolic techniques, and gives a unified point of view. This section also treats other researches on testing and observation of distributed programs.

**On-the-fly test synthesis :** We have designed on-the-fly test synthesis algorithms on systems models which operational semantics is a transition system with inputs, outputs and internal actions (IOLTS). Starting from an IOLTS specification model, test generation consists in extracting a visible sub-behavior (deterministic IOLTS without internal action). The on-the-fly test generation technique answers the state explosion problem
by extracting a test case using a test purpose that constrains the construction of a partial state space. While in other works (e.g. Tretmans) test generation and execution are done on-the-fly but lack of a real selection mechanism, our technique allows a better off-line selection of test cases. The main difficulty lies in efficient and complex algorithms that combine model-checking techniques with problems of partial observation and control. These algorithms have been implemented in the TGV tool which is now well known in the community. These works have impacted on several thesis in Irisa (P. Morel that I supervised) and elsewhere. Relative publications are [8, 24, 25, 53, 9, 31, 30, 15, 39].

Symbolic test synthesis: Since 2000 we study the test synthesis problem for extended automata models (IOSTS) which combine a control structure with unbounded data domains [35]. The semantics of such models is then an infinite state IOLTS. Off-line test synthesis can be formalized as extracting a sub-IOSTS (which semantics is a deterministic IOLTS). However, an exact analysis being not computable, test synthesis is performed using syntactic transformations based on approximate analysis with abstract interpretation. Test accuracy then depends on the precision of the analysis [44]. During test execution, constraint resolution is necessary to choose or check exchanged data values between the tester and the implementation. The algorithms have been implemented in the STG tool [36, 38].

Other works on testing: Combination of testing and verification in the enumerated case [43] and symbolic case [45]. Design of algorithms for testing asynchronous systems [32] for distribution of tests [27], for OO testing [29, 40], for the computation of integration strategies for systems with dependency cycles [33, 11].

Distributed observation: Based on partial order theory, we have designed techniques to verify at run-time some temporal properties of distributed programs [21]. Some current works on “monitoring” (e.g. G. Rosu in Urbana-Champaign) are very close to some of these ideas.

Diagnosis of discrete event systems: We recently proposed a generalization of the diagnosis problem for discrete event systems, based on a model of supervision patterns, a new formalization of the diagnosis problem in terms of required properties of the diagnoser, and algorithms for the construction of the diagnoser and the verification of diagnosability. A first version appeared in [56], a more elaborated one in [59].

Software and their distribution

See also http://www.irisa.fr/vertecs/software.html.

Jesar (1989-91): on-the-fly verification tool and unboundness test for communicating finite state machines. Approx. 5 kloc of Pascal. Solo designer and coder. Some algorithms have been transfered in Veda (Verilog) and ObjectGeode (Telelogic).

Viscope (1993): 3D drawing of state space. 10 kloc of Pascal and C. Main designer and coder (90%). Interfaced with CADP toolbox.


STG (2000-2006): Symbolic test generation and execution tool. Eperimemented on several case studies [37, 36]. Interfaced with the abstract interpretation tool NBAC. I participate in its design (algorithms and architecture). Approx. 10 kloc of C++. A new OCaml version is under development and will serve as a platform for the integration of works on test generation, diagnosis and control synthesis for symbolic transition systems.
Publications

Note: most references can be downloaded from my Web page http://www.irisa.fr/vertecs/Publis/Auteur/Thierry.Jeron.html

Thesis


Edited proceedings and book chapters


Articles (Referred Journals)


**French Journals**


**Other Articles**


**International Conferences (with program comittee)**


French-speaking Conferences (with program committee)


Recent research reports


Recent presentations and tutorials

Tutorials and invited lectures

- Invited lecture at the Summer School Movep, Nantes, 1996
- Tutorial for Greco (Paris), 1997,
- Invited lecture at Femsys (Munich), 1999.
- Tutorial at FM (Toulouse), 1999.
- Summer school Modelisation, Test and Validation (Marseille), 1999.
- Invited lecture for the review of the european projet VIRES (Autrans) in 2000,
- Tutorial for the School for Young Researchers in Programming (Rennes) in 2002
- Invited keynote speaker at FMCQ’06, Amsterdam, Nov. 2006.
Invited presentations

- Stanford Research Institute (SRI) in USA, 1999.
- University Rey Juan Carlos III in Madrid, 2000.
- CNR in Pisa, 2002.
- Irisatech, Irisa Rennes, 2002
- Labri in Bordeaux, 2004
- ENS Cachan Rennes, 2004
- Inria Industry, Rocquencourt, 2004
- DGA-Onera-Ensietaseminar, "Ingenierie des systemes complexes a logiciels preponderants", nov 2005
- ULB Bruxelles, dec 2005
- LIFC Besancon, dec 2005