Curriculum vitae

Thierry Jéron

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Personal information

Name:	Thierry Jéron
Date and place of birth:	June 7th, 1963, St Brieuc (France)
Citizenship:	French
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Education

- *Habilitation à diriger les recherches* in Computer Science, "Contribution à la génération automatique de tests pour les systèmes réactifs", University of Rennes 1 , march 16, 2004.
  Jury: R. Marie (Pres.), E. Brinksma, M.-C. Gaudel, A. Petrenko (Rapp.), R. Groz, C. Jard.
- Ph. D. in Computer Science, University of Rennes 1, mai 1991, "Contribution à la validation de protocoles : test d'infinitude et vérification à la volée".
  Jury: J. P. Banâtre (Pres.), A. Finkel, J. Sifakis (Rap.), M. Raynal, C. Jard, S. Graf, B. Algayres, P. Wolper.
- Master in Computer Science and Magister in Mathematical Modelisation and Computer Science Methods, 1988, University Rennes 1.

Professional Career

April 2001-Today: Research Scientist and Scientific Leader, VerTeCS research team, Irisa/Inria Rennes.

January 1993-April 2001: Research Scientist, Pampa research team, Irisa/Inria Rennes.

November 1991- December 1992: Engineer, Alcatel Alsthom Research Lab., Marcoussis.

June 1991- November 1991: Expert engineer, Pampa research team, Irisa/Inria Rennes

October 88 - May 91: Ph. D. Student, supervised by Claude Jard ADP research team, Irisa/Inria Rennes.

Ph. D. supervision and jury

Supervision of Ph. D. students

Yves-Marie Quemener: (93-96) "Vérification de protocoles à espace d'états infini représentables par une grammaire de graphes". Jury: J.-P. Banâtre (Pres.), A. Arnold, A. Bouajjani (Rapp.), O. Burkart, C. Jard, T. Jéron. Defended in November 1996. Heuristics allowing to finitely represent infinite state spaces of communicating finite state machines with graph grammars, model-checking of μ-calculus on this representation.

Pierre Morel: (96-2000) "Une algorithmique efficace pour la génération automatique de tests de conformité". Design of test generation algorithms and implementation in TGV. Jury: J.-P. Banâtre (Pres.), J.-C. Fernandez, R. Castanet (Rapp.), A. Kerbrat, C. Jard, T. Jéron.

Elena Zinovieva: (2000-2004) with V. Rusu. "Génération automatique de test de conformité par des techniques symboliques". Jury: O. Ridoux (Pres.), J. Tretmans, B. Legeard (Rapp.), C. Jard, B. Marre, V. Rusu. Formalization of symbolic test generation, design and development of STG.

Valery Tschaen (since 2001). "Modèles et techniques de la synthèse de tests et de la synthèse de contrôleur." Relations between test generation and controller synthesis.

Camille Constant (since 2004) with V. Rusu. "Vérification et test symboliques pour les systèmes réactifs". Combination of verification and symbolic test generation applied to voice services in the context of a France Telecom grant.

Tristan Le Gall (since 2004) with B. Jeannet. "Treillis abstrait pour le type de donnée "file d'attente" pour la vérification et la synthèse de contrôleurs". Verification of communication protocols by abstrat interpretation.

Hatem Hamdi (since 2005) with ENIS Sfax (Tunisie). "Test de la sécurité dans les réseaux". Automatic generation of network attacks from security policies.

Jeremy Dubreil (since 2006) "Formal methods for testing and supervision of security in networks"

Jury member of the dissertations of:

Gérard Cécé: "Vérification, analyse et approximations symboliques des automates communicants", ENS Cachan, January 1998 (co-reviewer with C. Jard).

Michel Bourdellès: "Analyse de systèmes réactifs à des fins de vérification : application au langage Esterel", University of Nice, May 1999 (reviewer).

Solofo Ramangalahy: "Test de conformité pour des spécifications à base d'automates : une approche par la théorie des jeux", University of Orléans, October 1999 (reviewer).

Manuel Aguilar: "Contribution à la validation de systèmes de processus communicants par files d'attente : analyse statique pour la réduction de files", University of Grenoble, December 2003 (reviewer).

Armelle Prigent: "Validation et tests formels: application à la conception d'architectures avioniques", Ecole Centrale de Nantes, December 2003.

Pierre Bontron: "Les schémas de test : une abstraction pour la génération de tests de conformité et la mesure de couverture", University of Grenoble, March 2005 (reviewer).

Hélène Le Guen: "Validation d'un logiciel par le test statistique d'usage: de la modélisation à la décision de livraison", University of Rennes, June 2005.

Cyril Pachon: Une approche basée sur les modèles pour le test de robustesse, University Joseph Fourier, Verimag, Grenoble, (rap), Octobre 2005 (reviewer).

Gregory Lestiennes: LRI Orsay, nov 2005

Franck Lebeau: Génération de tests à partir de statecharts fondée sur le calcul de comportements, University of Franche Comté, Besancon, 8 dec 2005 (reviewer).

Alban Gratien: Diagnostic décentralisé et en-ligne de systèmes à événements discrets reconfigurables, University of Rennes, 13 dec 2005.

Bram de Wachter: dSL, a Language and Environment for the Design of Distributed Industrial Controllers, Université Libre de Bruxelles (ULB), 2 and 16 December 2005.

Program committees

- Steering Committe of MOVEP 2006 (Bordeaux) and MOVEP 2004 (Bruxelles),
- Program Committee TACAS 2006 (Vienna, Tool Chair), and TACAS 2005 (Edinburgh),
- Program Committee TESTCOM 2006 (New-York), TESTCOM 2005 (Montréal), TESTCOM 2004 (Oxford),
- Program Committee FATES 2005 (Edinburgh), FATES 2004 (Linz), FATES 2003 (Montréal), co-chair of FATES 2002 (Brno), PC of FATES 2001 (Aalborg).
- Program Committee ROSATEA 2006 (ISSTA workshop, Portland),
- Program Committee LFM 2000 (Williamsburg, Virginia)
- Financial Chair of ISSRE 2004 (St Malo),

Grants and contracts

NB: marked with * are those grants and contracts in which I was the scientific leader for Irisa or the main contributor.

Grants relative to TGV

DGA-Vérilog (95)* : grant for DGA (Direction Générale de l'Armement) with Vérilog, Cap Sesa, le CNET, Célar, Vérimag and Irisa. Design and coding of the 1st version of TGV.

TestComposer (99)*: with Vérilog, le CNET, Vérimag and Irisa. Design, coding and experiment of TestComposer in the ObjectGéode toolbox (Verilog-Telelogic).

Forma (96-99)*: contract funded by CNRS and Research Ministry. Action with CNET, Vérimag, LSV (ENS Cachan), LaBri (Bordeaux). First connection of TGV with ObjectGéode and experiment on the SSCOP protocol.

GIE Bull Inria DYADE/VASY (96-2000): with Bull, the Vasy Inria team (Rhônes-Alpes). Adaptation of TGV for test synthesis for cache coherency protocols. Connexion of TGV to the CADP toolbox.

Van Gogh (99-2001)*: collaboration between Twente University and Irisa on test synthesis. Comparison of TGV and TorX on case studies.

RNTL COTE (2001-2002): with Softeam, FT R& D, Gemplus, AQL, LSR Imag and Irisa on testing for UML components. Definition of a UML profile for testing (impact on OMG's U2TP) and integration of TGV with Objecteering, Umlaut, Tobias and Casting.

European Project IST Agedis (2000-2004)*: IST European project with IBM Haifa (Israël) and IBM Hursley (G-B), Imbus (D), Intrasoft (Gr), FT R& D (Fr), University of Oxford (G-B), Vérimag and Irisa. Design and development of a toolbox for test synthesis and execution for UML distributed components. The test synthesis tool is an integration of Gotcha principles (IBM) in TGV.

Grants relative to symbolic testing and STG

Verdon (98-99)*: Inria action with Inria teams Vasy (Grenoble), Meije (Sophia), Pampa (Irisa) and LSR Imag. Treatment of data for verification and testing.

CP8/Schllumberger (2001)*: in the context of GIE Bull-Inria, then with a direct collaboration with CP8-Schlumberger, with the Vasy team. Symbolic test synthesis for smart-card applications. Design and coding of a first version of STG, experiments.

ARC Inria Modocop (2002-2004): Inria research action with Inria teams Lemme and Oasis (UR Sophia), Vasy (UR Rhône-Alpes), Verimag, LIFC (Besançon), Lande and VerTeCS (Irisa). Verification and testing for OO concurrent languages (Java and JavaCard) Comparison of STG with BZ-TT (LIFC) on the CEPS (electronic purse) case study.

CRE France Telecom (2004-2006)*: external research contract (CRE) funded by France Télécom R&D Lannion on testing of voice services. FTR&D already uses TGV-Agedis and wishes to use symbolic techniques for a better treatment of data.

European Network Artist2 (2004-2006): Network of Excellence on embedded systems. Partners of the Verification and Testing cluster with Aalborg (Danemark), Twente (Hollande), Liège and Bruxelles (Belgique), Verimag (Grenoble) and LSV (Cachan).

Grants relative to security

ACI Security Potestat (2004-2006)*: with LSR and Verimag (Grenoble), Landes and Distribcom Inria teams (Rennes). Using symbolic test generation techniques for the synthesis of network attacks.

RNRT Politess [2006-2008 *:] with LSR and Verimag (Grenoble), Distribcom Inria teams (Rennes), INT (Evry), Leyrios (Besançon), FTR&D (Caen), EnstB (Rennes), SAP Research(Paris), AQL Silicomp(Rennes). Security Policies for Network Information Systems: Modeling, Deployment, Testing and Supervision.

Grants relative to automotive

European Project Esprit Modistarc (97-99): with Dassault Électronique, and several manufacturers and academics. Test generation from SDL specifications of automotive applications.

AEE (99-2001)* and European Project EAST-EEA (2002-2004)*: French action (AEE) on Embedded Electronic Architectures and European follow-up (EAST-EEA) with European automotive industries. Design methodology for hardware and software embedded components.

Other grants

Véda: during my Ph. D., participation to a contract with Vérilog, France Télécom, Verimag and Irisa. Transfer of on-the-fly verification techniques in Véda (Vérilog). Re-used in its successor ObjectGéode (Telelogic).

Alcatel: during my stay in Alcatel, test of embedded systems in trains for GEC Alsthom, and European RACE project Specs (work on model-checking).

Working group Test-Objets: (99-2000) work group piloted by LAAS, LRI and Irisa on OO testing.

AS Testic*: (2002) research action with LAAS, LRI, LaBri, Vérimag and Irisa on robustness testing. **ACI Security V3F:** (2003-2005) with I3S (Nice), LIFC (Besançon), and CEA. Verification and testing for programmes with floating point numbers.

Collaboration Urbana-Verimag-Inria: (2005-2006) cooperation with Urbana Champaign and Verimag on runtime verification, monitoring, conformance testing and diagnosis.

Reviewing on projects proposals

- Open Technology Program of the Dutch Technology Foundation STW, 2005
- ARA SSIA and ACI SI, 2005
- RNTL, 2003, 2005
- Capes-Cofecub Franco-Bresilian cooperation

Responsabilities

- Scientific leader of Inria project team VerTeCS since 2001.
- Member of the Specialists Commissions of ENS Cachan (1998- 2003), and IFSIC-University Rennes 1 (2002-2004).
- Jury member for Inria research positions in Rennes (2003-2004)
- Jury member for secretary positions in Rennes (2002).
- Elected at the Lab Council from 88 to 91 (as Ph. D. student representative) and from 2000 to 2004 (as scientist representative).
- Elected at Inria Scientific Council (substitute) from 1997 to 2000.
- Responsible of the Irisa Monthly Seminar from 1997 to 2000.

Teaching

EnstB Rennes (3rd year): since 94, protocol validation, model-checking and testing.

EnstB Brest (2nd year): from 2001 to 2004, testing.

3xI Brest: from 95 to 96, protocol validation.

DIIC 3, University of Rennes: from 94 to 2003, protocol validation, model-checking and testing.

Master in Computer Science, University of Rennes:
From 2000 to 2002, computability and complexity.
From 2002 to 2006, testing (broadcasted to Lannion, Brest and Vannes from 2002 to 2005).

Summary of research activities

My research activity lies in the context of the validation of reactive systems. The main objective is to improve their reliability by using formal methods, i.e. founded on mathematical models and theories. More precisely, I have been interested in verification of properties on models (model-checking, control), and "dynamic" validation of real systems with respect to their models (e.g. observation, testing, diagnosis). This research goes from theory to practice: definition of models, formalization of validation problems, conception of algorithms and development of tools, transfer in academia and industry, and teaching of validation techniques. The most successful achievement is the conception of test generation algorithms developped in the TGV tool. Very novative when started, TGV has been quickly internationally recognized. It is still up to date and motivates other research on testing. Here after, I summarize the most significant research activities.

Verification

Verification consists in checking that a model of a system satisfies some properties. In this context, I have been interested in asynchronous systems modelled as communicating automata, with potentially infinite state spaces, and for which most problems are undecidable.

On-the-fly verification: We have conceived a generic algorithm for on-the-fly verfication, i.e. for verification during the construction of the state space of the model. This algorithm has been applied for model-checking linear temporal logic and for unboundness testing for communicating automata [18, 6]. The algorithm has been transfered in the Veda (Verilog) and ObjectGéode (Verilog/Telelogic) tools, two well known tools for the validation of telecommunication protocols.

Parallel verification: I have conceived a parallel verification algorithm for communicating automata, and implemented it on parallel machines. It is interested to see that such algorithms are still up-to-date with grids.

Verification of infinite state systems: During my Ph. D., I have conceived and implemented a semi-decision procedure (decision procedure for a well defined sub-class) for the unboundedness of automata communicating through fifo channels [19, 7]. Later I supervised the Ph. D. of Y.-M. Quemener (93-96), during which we extended this procedure in an algorithm that extracts a graph grammar finitely representing the infinite state space [26] and allows model-checking of CTL [23]. I now co-supervise Tristan Legall's Ph. D. On the same model, we propose a computation of an approximate reachability set based on abstract interpretation [57], and an extension for models with data.

Graphical "verification": I conceived and developped the Viscope tool which allows to represent state graphs of concurrent processes in 3 dimensions [22, 50], with an explicit representation of concurrency and sequentiality.

Control of discrete event systems: Control consists in ensuring that a (finite) model satisfies its properties by forbidding some controlable actions. In the context of V. Tschaen's Ph. D., we were interested in the relation between testing and controller synthesis. In [55, 41, 12] we showed how to ensure the conformance of an implementation with respect to its specification using control theory.

Dynamic validation

Since 95, most of my research concentrates on model-based conformance testing for non-deterministic reactive systems. In particular, we attack one of the most chalenging problem in testing, which is automatic test generation from formal models of systems. My habilitation document [2] focuses on these works for enumerative models and on-the-fly techniques, and on models with data with symbolic techniques, and gives a unified point of view. This section also treats other researches on testing and observation of distributed programs.

On-the-fly test synthesis : We have designed on-the-fly test synthesis algorithms on systems models which operational semantics is a transition system with inputs, outputs and internal actions (IOLTS). Starting from an IOLTS specification model, test generation consists in extracting a visible sub-behavior (deterministic IOLTS without internal action). The on-the-fly test generation technique answers the state explosion problem

by extracting a test case using a test purpose that constrains the construction of a partial state space. While in other works (e.g. Tretmans) test generation and execution are done on-the-fly but lack of a real selection mechanism, our technique allows a better off-line selection of test cases. The main difficulty lies in efficient and complex algorithms that combine model-checking techniques with problems of partial observation and control. These algorithms have been implemented in the TGV tool which is now well known in the community. These works have impacted on several thesis in Irisa (P. Morel that I supervised) and elsewhere. Relative publications are [8, 24, 25, 53, 9, 31, 30, 15, 39].

Symbolic test synthesis: Since 2000 we study the test synthesis problem for extended automata models (IOSTS) which combine a control structure with unbounded data domains [35]. The semantics of such models is then an infinite state IOLTS. Off-line test synthesis can be formalized as extracting a sub-IOSTS (which semantics is a deterministic IOLTS). However, an exact analysis being not computable, test synthesis is performed using syntactic transformations based on approximate analysis with abstract interpretation. Test accuracy then depends on the precision of the analysis [44]. During test execution, constraint resolution is necessary to choose or check echanged data values between the tester and the implementation. The algorithms have been implemented in the STG tool [36, 38].

Other works on testing : Combination of testing and verification in the enumerated case [43] and symbolic case [45]. Design of algorithms for testing asynchronous systems [32] for distribution of tests [27], for OO testing [29, 40], for the computation of integration strategies for systems with dependency cycles [33, 11].

Distributed observation: Based on partial order theory, we have designed techniques to verify at run-time some temporal properties of distributed programs [21] . Some current works on "monitoring" (e.g. G. Rosu in Urbana-Champaign) are very close to some of these ideas.

Diagnosis of discrete event systems: We recently proposed a generalization of the diagnosis problem for discrete event systems, based on a model of supervision patterns, a new formalization of the diagnosis problem in terms of required properties of the diagnoser, and algorithms for the construction of the diagnoser and the verification of diagnosability. A first version appeared in [56], a more elaborated one in [59].

Software and their distribution

See also `http://www.irisa.fr/vertecs/software.html`.

Jesar (1989-91) : on-the-fly verification tool and unboundness test for communicating finite state machines. Approx. 5 kloc of Pascal. Sole designer and coder. Some algorithms have been transfered in Véda (Verilog) and ObjectGéode (Telelogic)

Viscope (1993) : 3D drawing of state space. 10 kloc of Pascal and C. Main designer and coder (90%). Interfaced with CADP toolbox.

TGV (1995-2004) : on-the-fly test generation tool. Common with Verimag. Main designer of algorithms and tool architecture, developper of the first version, supervision of developments. 10 kloc of C. Works on Unix, Linux, Windows NT for SDL, UML, Lotos and IF specifications via interfaces with ObjectGéode for SDL, Caesar for Lotos, Umlaut for UML , IF.open for IF. Protected by no IDDDN.FR.001.310012.00.R.P.1997.000.20900. New version TGV-Agedis is curently under deposit. Distributed for academia in CADP toolbox (Vasy, Inria Rhônes-Alpes). Transfered in ObjectGéode (Telelogic). New version TGV-Agedis distributed in Agedis toolbox by IBM.

STG (2000-2006) : symbolic test generation and execution tool. Eperimented on several case studies [37, 36]. Interfaced with the abstract interpretation tool NBAC. I participate in its design (algorithms and architecture). Approx. 10 kloc of C++. A new O-Caml version is under development and will serve as a platform for the integration of works on test generation, diagnosis and control synthesis for symbolic transition systems.

Publications

Note : most references can be downloaded from my Web page
`http://www.irisa.fr/vertecs/Publis/Auteur/Thierry.Jeron.html`

Thesis

[1] T. Jéron. *Contribution à la validation des protocoles : test d'infinitude et vérification à la volée.* Thèse de doctorat, Université de Rennes I, May 1991.

[2] T. Jéron. *Contribution à la génération automatique de tests pour les systèmes réactifs.* Habilitation à diriger des recherches, Université de Rennes I, march 2004. http://www.irisa.fr/prive/jeron/HDR/doc_hdr_sent2.pdf.

Edited proceedings and book chapters

[3] R. Hierons and T. Jéron, editors. *FATES'02, Formal Approaches to Testing of Software, Brno, Czech Republic, A Satellite Workshop of CONCUR'02.* Inria Report, august 2002.

[4] F. Cassez, T. Jéron, F. Laroussinie, M. Ryan, and J.-F. Raskin, editors. *MOVEP2004, 6th School on Modeling and Verification of Parallel Processes, Brussels*, dec 2004.

[5] Camille Constant, Thierry Jéron, Hervé Marchand, and Vlad Rusu. *Combinaison entre vérification et test pour la validation de systèmes réactifs*, volume 1 of *Traité I2C, Systèmes Temps Réel : Techniques de Description et de Vérification - Théorie et Outils*, chapter 2. Hermès, 2006. À paraître.

Articles (Referred Journals)

[6] J.-C. Fernandez, C. Jard, T. Jéron, and L. Mounier. On-the-fly verification of finite transition systems. *Formal Methods in System Design*, 1(2-3):251–273, 1992.

[7] T. Jéron and C. Jard. Testing for unboundedness of fifo channels. *Theoretical Computer Science*, 113:93–117, 1993.

[8] J.-C. Fernandez, C. Jard, T. Jéron, and G. Viho. An experiment in automatic generation of conformance test suites for protocols with verification technology. *Science of Computer Programming*, 29:123–146, 1997. Egalement disponible en rapport de recherche Irisa n^o 1035 et Inria n^o 2923.

[9] M. Bozga, J.-C. Fernandez, L. Ghirvu, C. Jard, T. Jéron, A. Kerbrat, P. Morel, and L. Mounier. Verification and test generation for the SSCOP protocol. *Journal of Science of Computer Programming, special issue on Formal Methods in Industry*, 36(1):27–52, January 2000.

[10] C. Jard and T. Jéron. An educational case study in protocol verification and distributed observation. *Journal of Computer Science Education, ECASP Special Issue*, 10(3), 2000.

[11] Y. Le Traon, T. Jéron, J.-M. Jézéquel, and P. Morel. Efficient OO integration and regression testing. *IEEE Transactions on Reliability*, 49(1):12–25, March 2000.

[12] T. Jéron, H. Marchand, V. Rusu, and V. Tschaen. Ensuring the conformance of reactive discrete event systems by means of supervisory control. *International Journal Of Production Research (IJPR)*, 42(14):2809–2826, 2004.

[13] C. Jard and T. Jéron. TGV: theory, principles and algorithms a tool for the automatic synthesis of conformance test cases for non-deterministic reactive systems. *Software Tools for Technology Transfer (STTT), Special section on high-level test of complex systems*, 7(4):297–315, August 2005.

French Journals

[14] S. Ramangalahy, P. Le Gall, and T. Jéron. Une application de la théorie des jeux au test de conformité. *Revue Electronique sur les Réseaux et l'Informatique Répartie (RERIR)*, 9:3–23, mai 2000.

[15] T. Jéron. TGV: théorie, principes et algorithmes. *Techniques et Sciences Informatiques (TSI), Numéro spécial "Test de logiciel"*, 21(9):1265–1294, 2002.

Other Articles

[16] T. Jéron, C. Jard, C. Viho, B. Caillaud, H. Kahlouche, P. Morel, J.-C. Fernandez, A. Kerbrat, and M. Bozga. Génération automatique de tests pour les protocoles: l'exemple de l'approche formelle de TGV. *Revue de l'Electricité et de l'Eléctronique (REE)*, 3, March 1999.

International Conferences (with program commitee)

[17] C. Jard and T. Jéron. On-line model-checking for finite linear temporal logic specifications. In *Proceedings of the International Workshop on Automatic Verification Methods for Finite State Systems, Grenoble, France*, volume 407 of *LNCS*, pages 275–285. Springer–Verlag, June 1989.

[18] C. Jard and T. Jéron. Bounded memory algorithms for verification on the fly. In *CAV'91: Symposium on Computer Aided Verification, Aalborg, Denmark*, volume 575 of *LNCS*, pages 192–202. Springer Verlag, June 1991.

[19] T. Jéron. Testing for unboundedness of fifo channels. In *STACS 91 : Symposium on Theoretical Aspects of Computer Science, Hamburg, Germany*, volume 480 of *LNCS*, pages 322–333. Springer–Verlag, February 1991.

[20] T. Jéron. Prototype of a verification tool. In *STACS 91 : Symposium on Theoretical Aspects of Computer Science, Hamburg, Germany*, volume 480 of *LNCS*, pages 322–333. Springer–Verlag, February 1991. Tool demonstration.

[21] C. Jard, T. Jéron, G.-V. Jourdan, and J.-X. Rampon. A general approach to trace checking in distributed computing systems. In 14^{th} *International Conference on Distributed Computing Systems, Poznan, Pologne*, pages 396–403. IEEE Computer Society Press, June 1994.

[22] T. Jéron and C. Jard. 3D layout of reachability graphs of communicating processes. In *Graph Drawing: DIMACS International Workshop, GD'94, Princeton, New-Jersey, USA*, volume 894 of *LNCS*, pages 25–32. Springer-Verlag, October 1994. Egalement disponible en rapport de recherche bilingue français-anglais, Irisa n^o 852 et Inria n^o 2334, http://www.irisa.fr/bibli/publi/pi/1994/852/852.html.

[23] Y.-M. Quemener and T. Jéron. Model-checking of infinite Kripke structures defined by simple graph grammars. In A. Corradini and U. Montanari, editors, *SEGRAGRA'95, Joint COMPUGRAPH/SEMAGRAPH Workshop on Graph Rewriting and Computation, Volterra, Italie*, number 2 in ENTCS, pages 64–74. Elsevier Science B. V., September 1995. Egalement disponible en rapport de recherche Irisa n^o 927 et Inria n^o 2563.

[24] J.-C. Fernandez, C. Jard, T. Jéron, and G. Viho. Using on-the-fly verification techniques for the generation of test suites. In A. Alur and T. Henzinger, editors, *Conference on Computer-Aided Verification (CAV '96), New Brunswick, New Jersey, USA*, volume 1102 of *LNCS*. Springer-Verlag, July 1996. Egalement disponible en rapport de recherche Irisa n^o 1036, http://www.irisa.fr/vertecs/Publis/Ps/96-CAV-RR.ps.Z.

[25] L. Doldi, V. Encontre, J.-C. Fernandez, T. Jéron, S. Le Bricquir, N. Texier, and M. Phalippou. Assessment of automatic generation methods of conformance test suites in an industrial context. In B. Baumgarten and A. Burkhardt, H.-J.Giessler, editors, *IFIP TC6 9^{th} International Workshop on Testing of Communicating Systems*. Chapman & Hall, September 1996.

[26] Y.-M. Quemener and T. Jéron. Finitely representing infinite reachability graphs of CFSMs with graph grammars. In *FORTE/PSTV'96*. Chapman & Hall, October 1996. Egalement disponible en rapport de recherche Irisa n^o 994.

[27] C. Jard, T. Jéron, H. Kahlouche, and C. Viho. Towards automatic distribution of testers for distributed conformance testing. In *FORTE/PSTV'98, Paris, France*. Chapman & Hall, November 1998.

[28] C. Jard and T. Jéron. Verification and distributed observation of the alternating bit protocol. In *FORTE/PSTV'98, ECASP: Special Session on Educational Case Studies in Protocols*, Paris, France, November 1998.

[29] T. Jéron, J.-M. Jézéquel, and A. Le Guennec. Validation and test generation for object-oriented distributed software. In *IEEE Proc. Parallel and Distributed Software Engineering, PDSE'98, Kyoto, Japan*, April 1998.

[30] R. Groz, T. Jéron, and A. Kerbrat. Automated test generation from SDL specifications. In Rachida Dssouli, Gregor von Bochmann, and Yair Lahav, editors, *SDL'99 The Next Millenium, 9th SDL Forum, Montréal, Québec*, pages 135–152. Elsevier, June 1999.

[31] T. Jéron and P. Morel. Test generation derived from model-checking. In Nicolas Halbwachs and Doron Peled, editors, *CAV'99, Trento, Italy*, volume 1633 of *LNCS*, pages 108–122. Springer-Verlag, July 1999.

[32] C. Jard, T. Jéron, L. Tanguy, and C. Viho. Remote testing can be as powerful as local testing. In Jianping Wu, Samuel Chanson, and Qiang Gao, editors, *Formal methods for protocol engineering and distributed systems, FORTE XII/ PSTV XIX' 99, Beijing, China*, pages 25–40. Kluwer Academic Publishers, October 1999.

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French-speaking Conferences (with program commitee)

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Recent research reports

[57] Bertrand Jeannet, Thierry Jéron, and Tristan Le Gall. Abstract interpretation of FIFO channels. Technical Report 5784, Inria, December 2005. Also Irisa report n^o 1767.

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Recent presentations and tutorials

Tutorials and invited lectures

- Invited lecture at the Summer School Movep, Nantes, 1996
- Tutorial for Greco (Paris), 1997,
- Invited lecture at Femsys (Munich), 1999.
- Tutorial at FM (Toulouse), 1999.
- Summer school Modelisation, Test and Validation (Marseille), 1999.
- Invited lecture at the Dutch Testing Day (Eindhoven), 1999.
- Invited lecture for the review of the european projet VIRES (Autrans) in 2000,
- Tutorial for the School EDF-INRIA on Formal Methods (Paris), 2000.
- Tutorial for the School for Young Researchers in Programming (Rennes) in 2002
- Tutorial for the School on Real-Time (Toulouse) in 2003.
- Lecture on Model-based testing at Artist2 Summer School on Component & Modelling, Testing & Verification, and Statical Analysis of Embedded Systems, Sept. 29 - Oct. 2, 2005.
- Invited talk at DIPES'06, Braga (Portugal), Oct. 2006.
- Invited keynote speaker at FMCO'06, Amsterdam, Nov. 2006.

Invited presentations

- LITP in Paris, 1997.
- LSV Cachan, 1997.
- Lami, University of Evry, 1997.
- FT R & D Lannion, 1997.
- Stanford Research Institute (SRI) in USA, 1999.
- University Rey Juan Carlos III in Madrid, 2000.
- CNR in Pisa, 2002.
- Irisatech, Irisa Rennes, 2002
- Labri in Bordeaux, 2004
- ENS Cachan Rennes, 2004
- Inria Industry, Rocquencourt, 2004
- DGA-Onera-Ensieta seminar, " Ingenierie des systemes complexes a logiciels preponderants ", nov 2005
- ULB Bruxelles, dec 2005
- LIFC Besancon, dec 2005