# JUNIER Aurore

IRISA, Campus de Beaulieu, F-35042 Rennes Cedex France
24 years old
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## Field of competence:

- Computer science:
  - Logique and automata
  - Networks, systems and architecture
  - programming languages (Java, C, C++, Caml) and compilers
- Telecommunication:
  - Signals processing
  - Electricity
  - Electromagnetism
- Mathematics:
  - Markov Chain
  - Probability/Statistics
- English: TOEIC (830 points)

## Education:

2008 - 2010: Master Degree in Computer Science and Telecommunication oriented to reserch, ENS, Cachan, Brittany
2008 – 2009 : Master 1st year in computer science and telecommunication ENS Cachan, Bretagne
2007 – 2008: Bachelor's degree in Computer science
2005 - 2007**:** 2-year university cycle, University of Rennes, France

## Relevant Work Experience:

2010 : Internship in Distribcom laboratory with Anne Bouillard, IRISA, Rennes "Computing deterministic performance bound for network with fix priorities service policy".

Summer 2009: Internship in Computer Science 12, Heiko Falk, TU Dortmund, Germany, "ILP-based WCET aware register allocation".

One of the most important optimization of a compiler is register allocation. Most of compilers decide where and when to spill code without know the implication of these load/store on the execution of a program. **We are going** to extend an ILP-based compiler with a better WCET estimation.

2008 – 2009: Chief of the Master's first year project: « C2Silicium »

In embedded systems, it is an actual necessity to realise calculi as fast as possible. In order to accelerate calculi that are difficult for CPU, computer scientists often use dedicated components. However it is difficult to do this kind of component. We created the « C2Silicium » software that, taken the C

code of a program, is able to give the definition of a dedicated component to realise.

Summer 2008: Internship in the CAPS group (*www.irisa.fr/caps*/), IRISA (*www.irisa.fr*) Rennes, France, Statistic WCET estimation: study of the impact of cache replacement policies on the tightness of WCET estimation.

There is a need of considering caches when validating the temporal behaviour of the real time systems in particular when estimating task's WCET. We have used new theoretical results to improve a static instruction cache analysis method for set-associative instruction caches with a Pseudo-LRU and random replacement policies.

## Publication:

2008: Impact of cache replacement policy on the tightness of Worst Case Execution Time estimation, Damien Hardy, Isabelle Puaut,
Poster presentation in the Workshop : Real Time and Network Systems 2008 (rtns08.inria.fr)

## Work experience:

2009 – 2010: Computer science teacher for first year at university of Rennes
2004 – 2010 : Give private lessons in mathematics and physic for college
2004 – 2007: Waitress in a restaurant during the summer 2007
Waitress in a gala organized by an association in summers
Baby sitting all Saturday morning

## Miscellaneous information:

Work in a charitable association for children
Practice Ballrooms dance
Driving License
English (curant)
German (scolaire)