



Multiple Valued Logic - MVL

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What is MVL?

- Currently, computers and other electronic devices run as 101101... binary logic with 2 logical states: 0, 1
- Multivalued logic offers many logical states: 0, 1, 2, 3, 4,5 ... and more complex functions in less time and space than binary applications
- Until the SUS-LOC technology was developed, MVL was impractical or unachievable through conventional means, and drew only theoreticians and researchers looking for the key to making it usable
- SUS-LOC was invented in the 1990's by Dan Olson and is proving to be the long sought solution

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Technical advantages of SUS-LOC MVL circuits and devices

- A decrease in required power
- A decrease of passive parasitic values
- Ability to perform multiple logic functions in one operation
 - e.g. $(A+B) \text{ AND } D$
- An increase in data density
- Reduced package size due to fewer required pins
- Superior performance (more bandwidth) with a reduced clock rate
 - 1 Mbit/s = 125 kbyte/s
 - 1 byte = 5-6 ternary digit
 - 750 ktit/s

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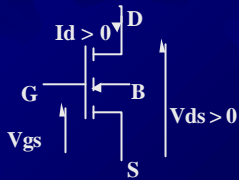
Introduction

- Les bases pour aborder la MVL
- Les fonctions à 1 entrée
- Les fonctions à 2 entrées

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Transistors à enrichissements

Le MOSFET à enrichissement avec un canal N



Conduction : $V_{gs} > V_{t_n} > 0$
e.g. 0.45V

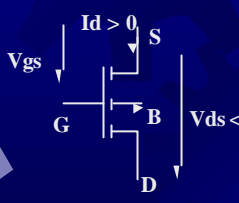
Quand la Source est reliée au Bulk



En logique binaire



Le MOSFET à enrichissement avec un canal P



Conduction : $V_{gs} < V_{t_p} < 0$
e.g. -0.45V

Quand la Source est reliée au Bulk

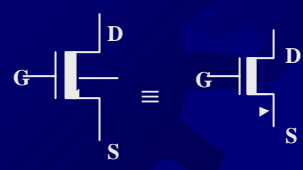


En logique binaire



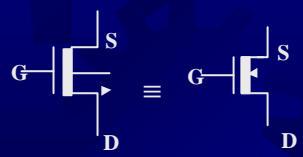
Les transistors à appauvrissements

Le MOSFET à appauvrissement avec un canal N



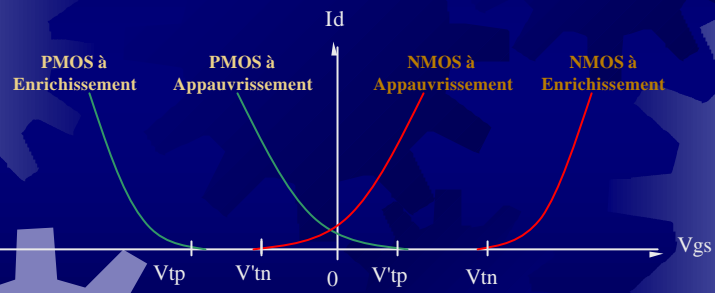
Conduction : $V_{gs} > V_{t_n} < 0$
e.g. -0.45V

Le MOSFET à appauvrissement avec un canal P



Conduction : $V_{gs} < V_{t_p} > 0$
e.g. 0.45V

Les caractéristiques : $I_d = F(V_{gs})$



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Number representation

Decimal	Binary			Ternary	
	Z	Y	X	W	V
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	2
3	0	1	1	1	0
4	1	0	0	1	1
5	1	0	1	1	2
6	1	1	0	2	0
7	1	1	1	2	1
8	#####	#####	#####	2	2
9	#####	#####	#####	#####	#####

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Les Fonctions à 1 entrée

- ☀ Les fonctions élémentaires
- ☀ L'inverseur binaire
- ☀ L'inverseur ternaire

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Les fonctions élémentaires

- ☀ Les fonctions logiques binaires

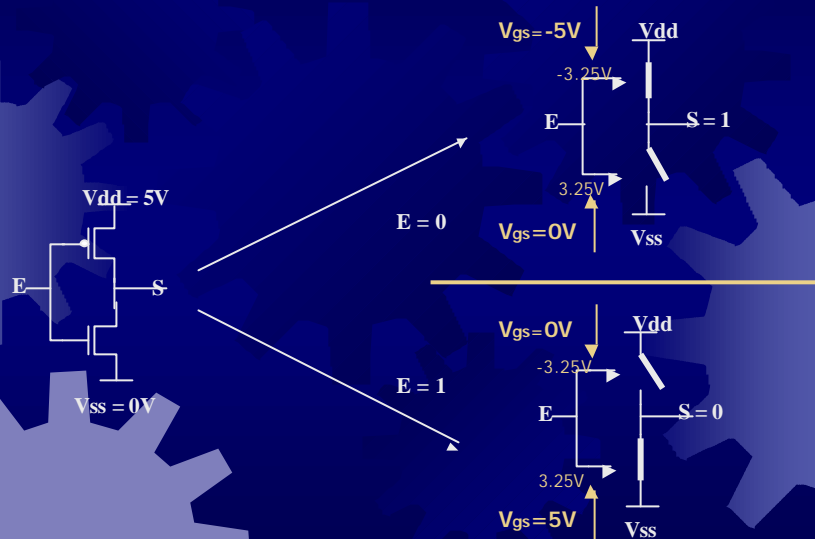
X	E ₀	Id	Not	E ₁
0	0	0	1	1
1	0	1	0	1

- ☀ Des fonctions logiques ternaires (27)

X	E ₀	E ₁	E ₂	C ₀	C ₁	C ₂	N(x)	Id(x)
0	0	1	2	2	0	0	2	0
1	0	1	2	0	2	0	1	1
2	0	1	2	0	0	2	0	2

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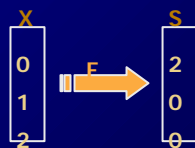
L'inverseur binaire



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La logique 3 valeurs

• $F(x) = \langle 2 \ 0 \ 0 \rangle = C0(x)$

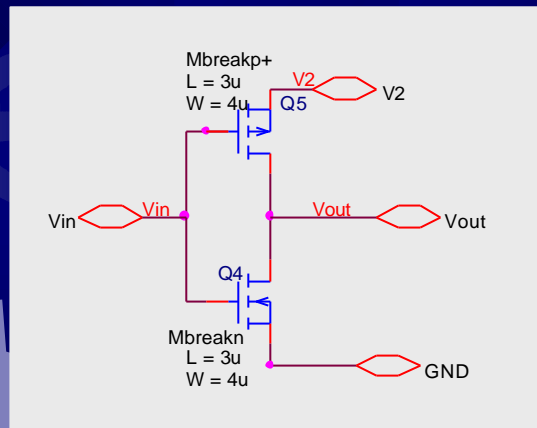


• Différentes négations

X	$N(x) = \langle 2 \ 1 \ 0 \rangle$	$C0(x) = \langle 2 \ 2 \ 0 \rangle$
0	2	2
1	1	2
2	0	0

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C₀



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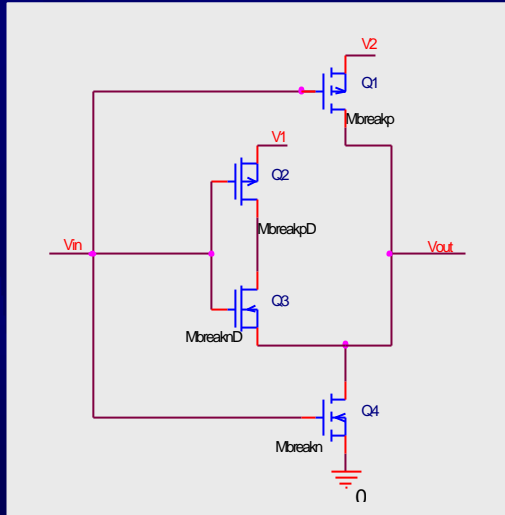
The three requirements of SUS-LOC:

- There must be one controllable path, or branch, from a source of power to an output terminal of a circuit, per output logic level
- Only one controllable path, or branch, conducts from a source of power to an output terminal per input logic level, contiguous group of input logic levels, or unique combination of input logic levels
- There must be « r » different sources of power, each source of power represents only one of « r » different logic levels

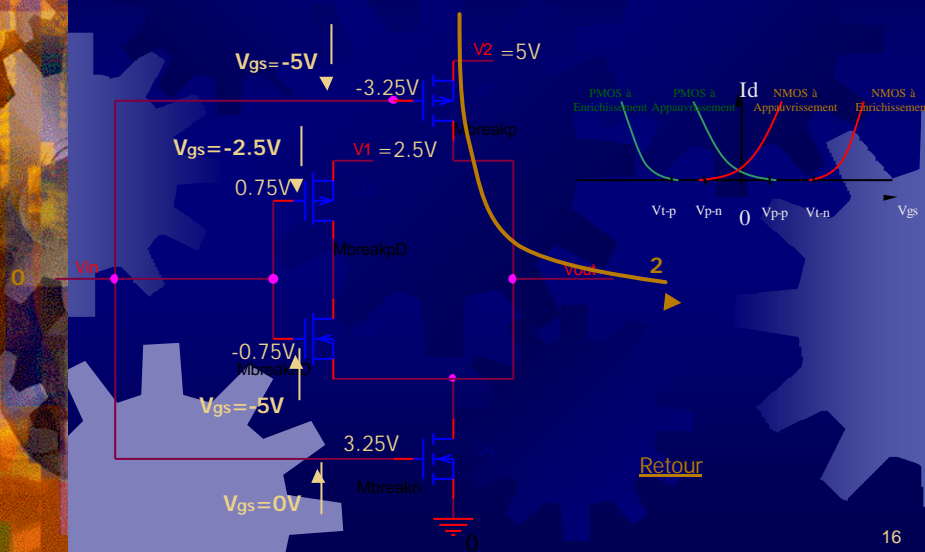
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Inverseur 3-VL

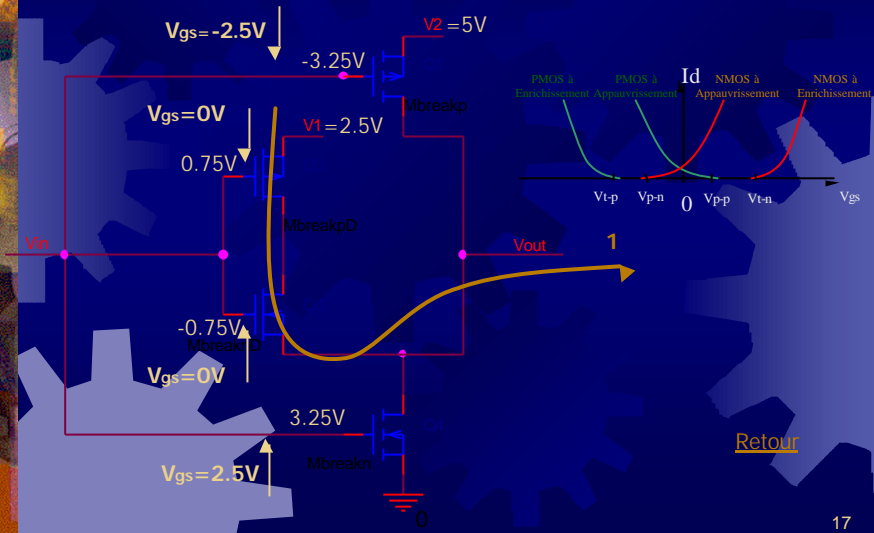
- ☀ $V_{in} = 0$
 - [Figure 5](#)
- ☀ $V_{in} = 1$
 - [Figure 6](#)
- ☀ $V_{in} = 2$
 - [Figure 7](#)



Inverseur 3-VL - $V_{in}=0$

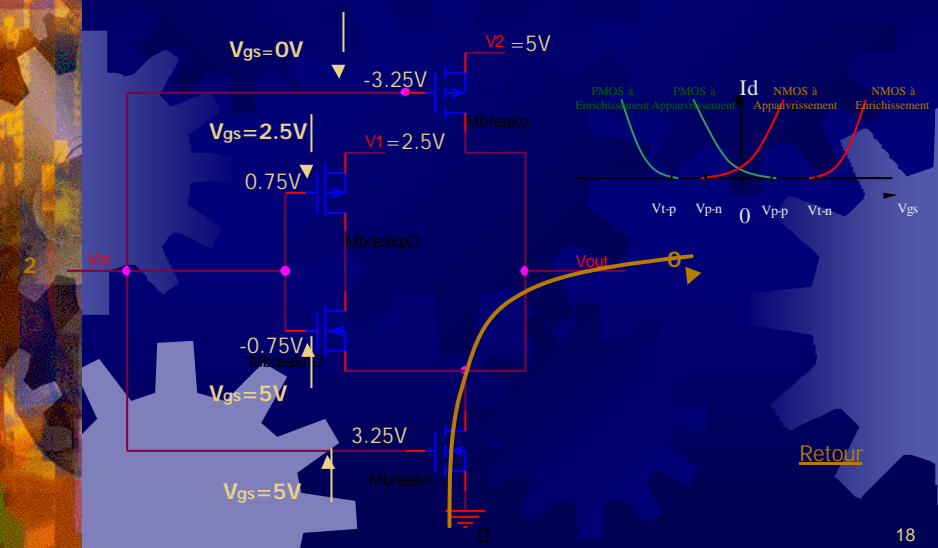


Inverseur 3-VL - $V_{in}=1$



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Inverseur 3-VL - $V_{in}=2$



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Inverter delay and Power

- ☀ 0.25 micron technology

- CI = 5fF
- ELDO simulator

Binary			Ternary		
	delay	power		delay	power
0->1	80ps	3,1 uW	2->1	140ps	470 nW
1->0	80ps	265 nW	1->2	85ps	970 nW
			2->0	160ps	411 nW
			0->1	110ps	436 nW
			1->0	82ps	35 nW
			0->2	142ps	1,5 uW

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Les Fonctions à 2 Entrées

- ☀ ET/OU

- $X.Y = \text{MIN}(X,Y)$
- $X+Y = \text{MAX}(X,Y)$
 - Associativité, commutativité
 - $C0(X+Y) = C0(X).C0(Y)$
 - $C0(X.Y) = C0(X)+C0(Y)$
- Idem avec N(x)
- A plus B, N(A plus B)

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Les Fonctions à 2 Entrées

Etude de la fonction $CGAND_3$ ($\equiv NAND_2$)
(CGAND = Complementing Generalized AND)



	A		
	0	1	2
0	2	2	2
1	2	1	1
2	2	1	0

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La fonction $CGAND_3$

- ✦ Définir les paramètres du circuit
- ✦ Développer le tableau de Karnaugh
- ✦ Déterminer les liens logiques entre les entrées et la sortie
- ✦ Concevoir le circuit

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Etape 1 - CGAND

- Logique ternaire [0 1 2]

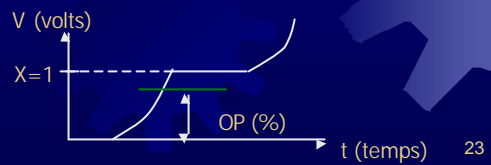
$V_0 = 0$ Volts

$V_1 = 2.5$ Volts

$V_2 = 5$ Volts

LSV = 2.5 Volts (Logic Step Voltage)

OP = 70 % (Overlap Percentage)



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Etape 2 - CGAND

		A		
		0	1	2
B	0	2	2	2
	1	2	1	1
	2	2	1	0

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Etape 3 - CGAND

A	B	S	A	B	S	A	B	S
0	0	2	0	1	2	0	2	2
1	0	2	1	1	1	1	2	1
2	0	2	2	1	1	2	2	0

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Etape 3 - CGAND

A	B	S
= 0	x	= 2
x	= 0	= 2
= 1	≥ 1	= 1
≥ 1	= 1	= 1
= 2	= 2	= 0

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Etape 4 - CGAND

☀ Branches extrêmes

- $E > S$: canal NMOS
- $E < S$: canal PMOS

☀ Branches intermédiaires

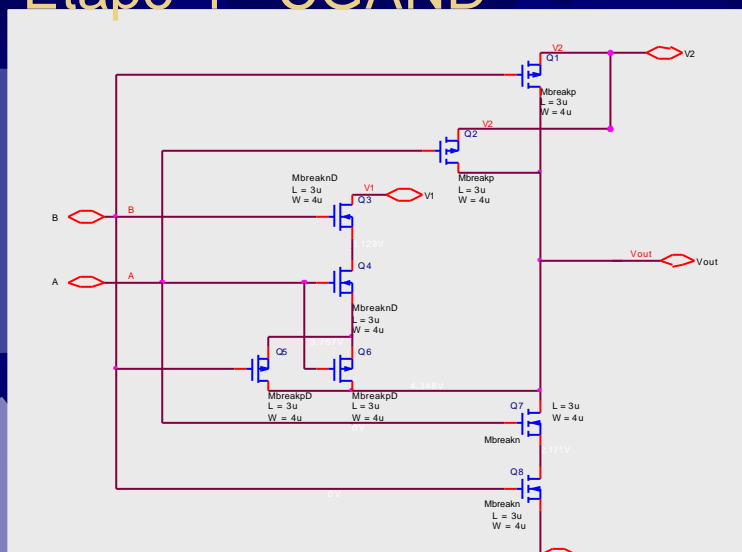
- $E < S$: canal PMOS E et NMOS D
- $E = S$: canal PMOS D et NMOS D
- $E > S$: canal PMOS D et NMOS E

☀ $V_{tn} = V_i - (V_o + (OP * LSV))$: transistor N

☀ $V_{tp} = V_i - (V_o - (OP * LSV))$: transistor P

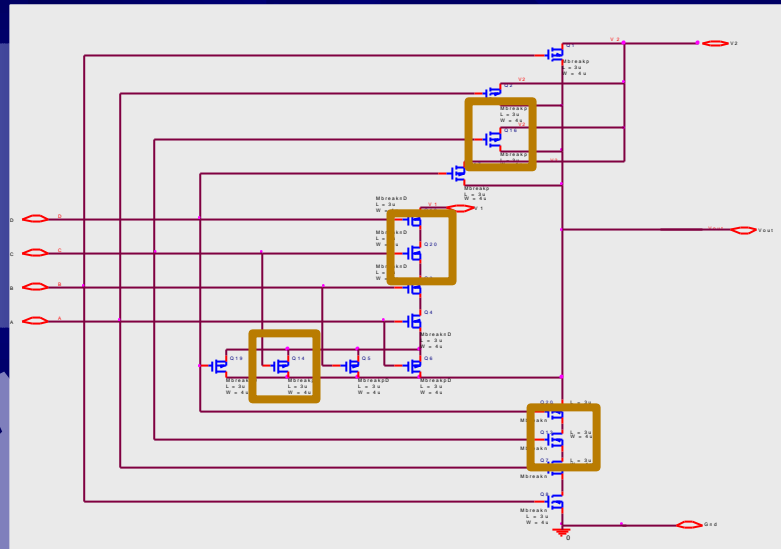
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Etape 4 - CGAND



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Etape 4 - CGAND



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Additionneur ternaire

- ☀ Equations logiques
 - Logique binaire
 - Logique ternaire
- ☀ Complexité

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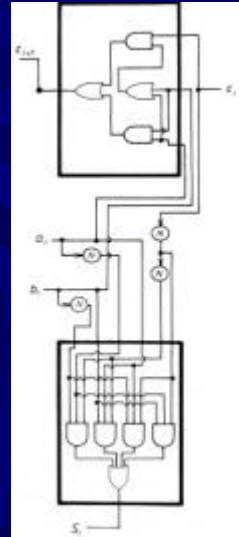
Logique binaire

a_i	b_i	c_i	S_i	c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S_i = \overline{a_i} \overline{b_i} \overline{c_i} \vee \overline{a_i} \overline{b_i} c_i \vee \overline{a_i} b_i \overline{c_i} \vee \overline{a_i} b_i c_i$$

$$c_{i+1} = \overline{a_i} b_i c_i \vee a_i \overline{b_i} c_i \vee a_i b_i \overline{c_i} \vee a_i b_i c_i$$

$$c_{i+1} = a_i b_i \vee a_i c_i \vee b_i c_i$$



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Logique ternaire

a_i	b_i	c_i	S_i	c_{i+1}
0	0	0	0	0
0	1	0	1	0
0	2	0	2	0
1	0	0	1	0
1	1	0	2	0
1	2	0	0	1
2	0	0	2	0
2	1	0	0	1
2	2	0	1	1
0	0	1	1	0
0	1	1	2	0
0	2	1	0	1
1	0	1	2	0
1	1	1	0	1
1	2	1	1	1
2	0	1	0	1
2	1	1	1	1
2	2	1	2	1

$$S_i = e_i C_0(a_i) C_1(b_i) C_0(c_i)$$

$$\vee e_i C_1(a_i) C_0(b_i) C_0(c_i)$$

$$\vee e_i C_2(a_i) C_2(b_i) C_0(c_i)$$

$$\vee e_i C_0(a_i) C_0(b_i) C_1(c_i)$$

$$\vee e_i C_1(a_i) C_2(b_i) C_1(c_i)$$

$$\vee e_i C_2(a_i) C_1(b_i) C_1(c_i)$$

$$\vee C_0(a_i) C_2(b_i) C_0(c_i)$$

$$\vee C_1(a_i) C_1(b_i) C_0(c_i)$$

$$\vee C_2(a_i) C_0(b_i) C_0(c_i)$$

$$\vee C_0(a_i) C_1(b_i) C_1(c_i)$$

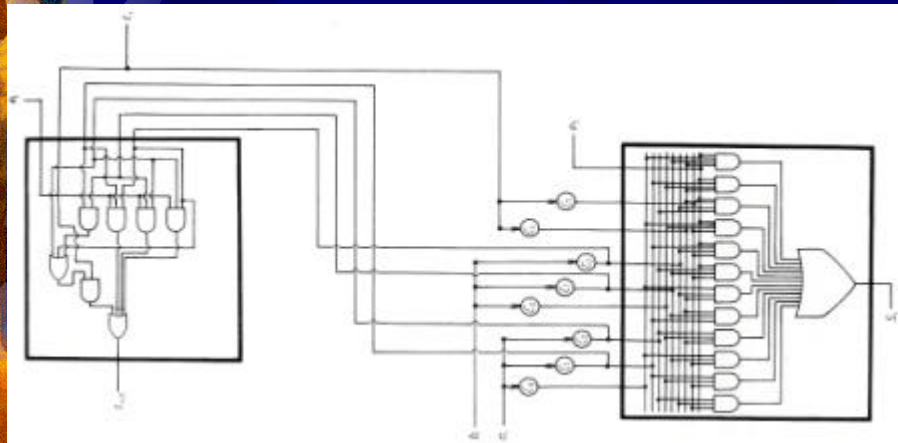
$$\vee C_1(a_i) C_0(b_i) C_1(c_i)$$

$$\vee C_2(a_i) C_2(b_i) C_1(c_i)$$

$$c_{i+1} = e_i [C_1(a_i) C_2(b_i) \vee C_2(a_i) C_1(b_i) \vee C_2(a_i) C_2(b_i)] \vee c_i [C_2(b_i) \vee C_1(a_i) C_1(b_i) \vee C_2(a_i)]$$

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Logique ternaire



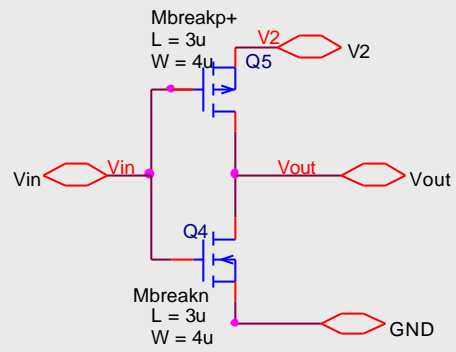
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Additionneur ternaire

- ☀ Optimisation FA ternaire
 - A plus B
 - A plus B plus carry
 - A plus B plus C plus carry
- ☀ Comparaison avec binaire
 - Binaire : adder 16 bits
 - Ternary : adder 10 *tits*

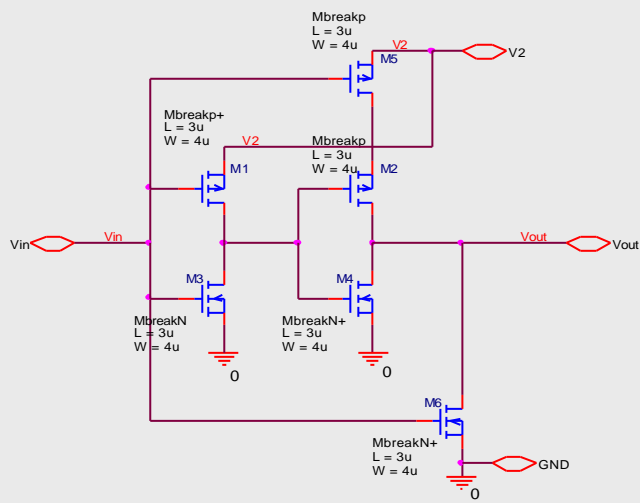
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C₀



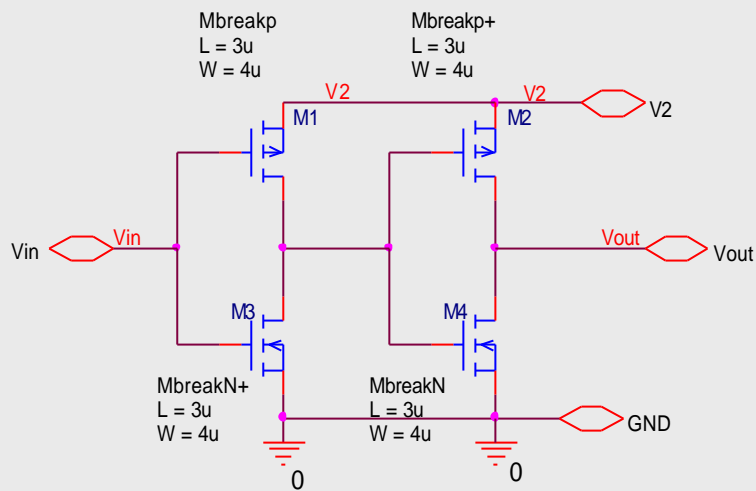
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C₁



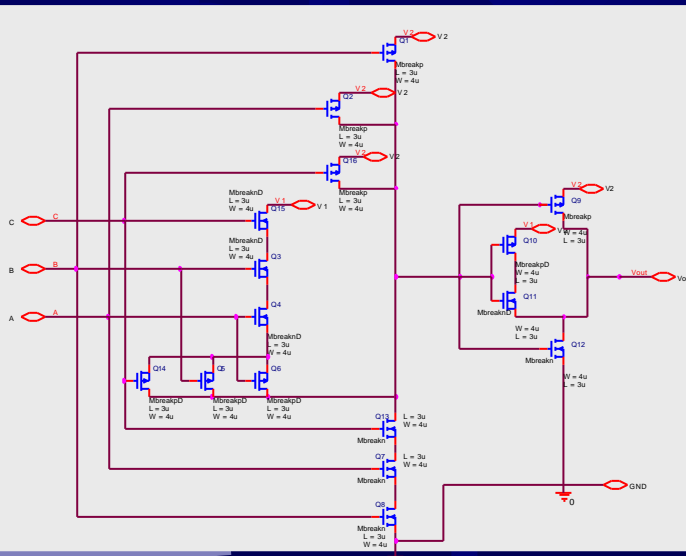
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C₂



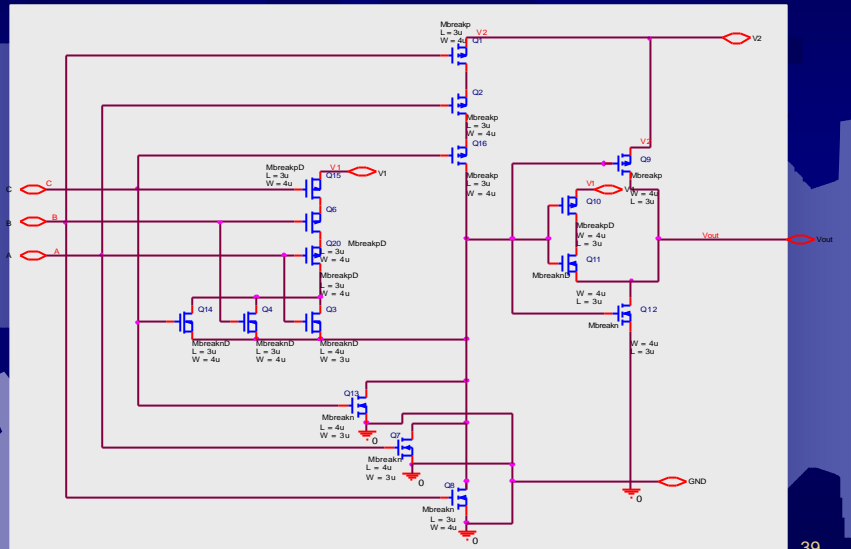
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AND à 3 entrées



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OR à 3 entrées



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Goal of our project

- ☀ Demonstration of the SUS-LOC technology efficiency for MVL (3L, 4L)
 - Power-Speed Efficiency
- ☀ Telecommunication application context
- ☀ Digital Signal Processor Architecture
 - Dedicated Processing Unit (arithmetic unit, hard-wired multiplier, register file)
 - Internal Memories (ROM, RAM)
 - Simple control model

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Schedule (1)

- ☀ Study the power-speed efficiency of SUS-LOC circuits on representative blocks (arithmetic, memory, etc.)
- ☀ Ternary and Quaternary Logic
- ☀ Compare the results with their equivalent in binary
 - ☑ Adder
 - ☐ Multiplier
 - ☐ Register

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Schedule (2)

- ☀ Definition of a library of SUS-LOC standard cells at the transistor level (flip-flop, latch, logic gates, arithmetic functions, multiplexer).
 - Characterization in terms of power, speed, area
- ☀ Definition of VHDL-based models of SUS-LOC standard cells at the gate (and transistor ?) level.

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Schedule (3)

- ☀ Design of typical arithmetic and logic elements of a DSP (multiplier, ALU, barrel shifter, register files).
- ☀ Design of a Digital Signal Processor.
 - VHDL based design
 - Simulation for verification
 - Simulation for characterization
- ☀ Definition of a CAD tool for designing SUS-LOC structures

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What we have done

- ☀ Design of basic SUS-LOC structures using Spice models
 - Ternary Full-Adder
- ☀ Porting of the structures in STM 0.25 μ technology (depletion transistors extrapolated)
- ☀ Definition of a VHDL package for simulation
 - "STD_TERNARY_LOGIC"

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Research directions

- ✦ Logic Synthesis and Mapping for MVL and SUS/LOC
 - SIS/MVSIS (UCB)
- ✦ CAD Tools
- ✦ Technology
 - SOI, new transistors
- ✦ Communications in higher radix than 2