Post-doc

Title: Accuracy Aware SIMD instruction selection & scheduling

Keywords and skills: optimizing compilers, automatic parallelization, processor architecture, multi-core platforms, numerical accuracy, digital signal processing

Duration: 12 month (renewable once)

Laboratory: IRISA/INRIA – CAIRN project-team

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Current and future wireless communication and video standards have huge processing power requirements, which cannot be satisfied with current embedded single processor platforms. Most platforms now therefore integrate several processing core within a single chip (see ARM Cortex-A9 for example), leading to what is known as embedded multi-core platforms. This trend will continue, and embedded system design will soon have to implement their systems on platforms comprising tens if not hundred of high performance processing cores. Examples of such architectures are the Xentium processor from by Recore [1] or the Kahrisma processor, a radically new concept of morphable processor from Karlsruhe Institute of Technology (KIT) [2].

This evolution will obviously pose significant design challenges, as parallel programming is notoriously difficult, even for domain experts. In the context of the FP7 European Project Alma (Architecture oriented parallelization for high performance embedded Multi-core systems using scilAb) [3], we are studying how to help designers programming these platforms by allowing them to start from a specification in Matlab and/or Scilab, which are widely used for prototyping image/video and wireless communication applications.

Because these languages use floating-point arithmetic, these initial specifications must be manually converted to a second version (usually in C) based on fixed-point arithmetic (floating point units are slow and use more power than integer units). This modified version then serves as a reference program that will be parallelized and mapped on the target platform. In practice, it turns out that the floating-point to fixed-point conversion step involves many implementation choices, which may in turn hinder interesting parallelization opportunities (e.g. through short-width SIMD extension such as ARM Neon extensions [4]).

The goal of the Post-doc is therefore to explore how to adapt existing SIMD instruction selection and scheduling algorithms to integrate the possibility of using different fixed-point data encodings for each variable. The thesis work will leverage the expertise on the CAIRN team on both instruction selection and scheduling techniques for application specific processors [5,6] and automatic floating-point to fixed-point conversion [7].