IRISA • Campus universitaire de Beaulieu • 35042 Rennes Cedex France • Tél. : +33 2 99 84 71 00 • Télécopie : +33 2 99 84 71 71 • Internet : www.irisa.fr

PhD proposal

Laboratory: IRISA/INRIA – Cairn team
Place: Lannion, France

Title: Systems performances fixed-point arithmetic
Keywords : fixed-point arithmetic, quantization noise, embedded systems, digital communications.

Supervisor: Olivier Sentieys olivier.sentieys@irisa.fr
Co-supervisor: Romuald Rocher romuald.rocher@irisa.fr
Co-supervisor: Daniel Ménard daniel.menard@irisa.fr

Subject

Digital signal processing applications are specified with floating-point data types to prevent problems due to computing accuracy and overflows. However, to satisfy cost constraints and energy consumption, application implementation in embedded systems requires fixed-point arithmetic. Thus, the floating-point application must be converted into a fixed-point specification.

Fixed-point arithmetic formats are composed of an integer part and a fractional part. Thus, the fixed-point conversion process is divided into two steps. First, the binary-point position is defined using data dynamic range. This determines integer part word-length of all data inside the application in order to prevent overflows. Then, fractional part introduces an unavoidable quantization noise. These different quantization noise sources are propagated through the system and lead to an output quantization noise which modifies application computing quality. Computing accuracy damages must be contained to ensure algorithm integrity and application performances. So, accuracy evaluation is an important step of floating-point to fixed-point process.

In CAIRN team, we develop a tool to automate floating-point to fixed-point conversion, in order to reduce application time-to-market. This tool aims at defining an optimized fixed-point specification from the floating-point application description [1]. This optimization must minimize the implementation cost under accuracy constraint. For a software implementation, the cost represents the algorithm execution time. For a hardware implementation, the cost can be the energy consumption or the architecture area. The constraint is the computing accuracy. The computing accuracy is determined analytically to reduce significantly optimization time [2]. This method is defined for arithmetic operations (additions, multiplications, subtractions and divisions) for signal processing systems. This quality can be defined as Signal to Quantization Noise Ration (SQNR) or Bit Error Rate (BER) for digital communications.

One important step during fixed-point conversion is quality evaluation. An analytical approach has ever been developed for arithmetic operators. The aim of this project is to extend the method to decision operators. These operators are presented in many telecommunications systems such as turbo-codes and synchronization systems. An error in a decision due to fixed-point arithmetic will modify system behavior. So, it is necessary to control them to obtain a desired BER. This thesis will be applied on telecommunications applications to evaluate their performances

This thesis will be situated in Lannion

References

[1] D. Menard, “Méthodologie de compilation d’algorithmes de traitement du signal pour les processeurs en virgule fixe sous contrainte de précision” Thèse, décembre 2002.

[2] R. Rocher, D. Menard, O. Sentieys and P. Scalart, "Analytical accuracy evaluation of Fixed-Point Systems", In the proceedings of the EUSIPCO 2007, pp. 999-1003, September 2007, Poznan.