

Master de Recherche – Master of Research

- Title:** Design of fault-tolerant coarse-grained reconfigurable architectures through self-reconfiguration
- Keywords:** coarse-grained reconfigurable computing, embedded system, fault-tolerant computing (FTC), reconfigurable system
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Embedded systems permeate our everyday lives and we increasingly depend upon them to operate as expected. Because people count on these systems to operate as expected, special care must be taken to ensure that they are dependable (in particular, safe and reliable). Safety in the context of embedded systems deals with minimizing the frequency of mishaps (especially loss of life, injuries, and damage to property). Dependable computing systems for critical applications are generally real-time systems, such as those used in cars, avionics (fly-by-wire), nuclear reactor control, communication platforms, and remote applications - space stations and satellites, which should work correctly in harsh environments (exposition to radiation, electromagnetic noise, etc.) which could cause temporary or permanent faults.

Indeed for a few years, designers of critical terrestrial applications must consider the effects of high-energy charged particles (radiation) on electronic components. In particular, reconfigurable systems are concerned with the effects of single-event upsets (SEUs) induced by cosmic rays on configuration memory of a reconfigurable system. Changes to configuration memory can cause changes in the functionality and performance of the device. Since the cause of the failure is actually transient, on-line reconfiguration is sufficient to restore the original functionality. In the case of permanent faults, and after the faulty elements are located - either configurable logic blocks (CLBs) or routing resources - they must be excluded and replaced by previously unused fault-free resources.

Today's reconfigurable architectures enable partial and dynamic run-time self-reconfiguration. This feature allows the substitution of parts of a hardware design implemented on this reconfigurable hardware, and therefore, a single device can be adapted to implement various functionalities actually demanded, by simply uploading a new configuration. Reconfigurable hardware is useful in the design of dependable computing systems since runtime reconfiguration allows either to adapt the functionality of a system to the current needs or to tolerate its internal faults. In the latter case, the replacement of faulty resources can be accomplished by reprogramming the device with an alternative configuration that preserves the logical functionality utilizing a set of fault-free resources and excluding the faulty ones. The advantage of a self-reconfigurable system is that it can modify its own configuration without using additional external components.

The aim of this Master's thesis is to study various approaches aimed at improving the dependability of coarse-grained reconfigurable architectures. Some of them are (but not limited to): on-line error detection and/or correction techniques during system operation, techniques for very fast fault location, recovery methods from temporary faults, and permanent-fault repair methods through reconfiguration. The topics of this study insert well into the research activities of the CAIRN Team concentrated around dynamically reconfigurable architectures and dependable computing. The DART reconfigurable architecture developed by CAIRN Team (described in [2]) will serve as a vehicle to develop and implement some specific design methods for fault-tolerance.

References

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