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Master de Recherche – Master of Research

Title: Dynamic Voltage Scaling and Power Gating in SRAM Memory Structure for Low-Power Embedded FPGAs.

Keywords: power consumption, SRAM, FPGA, voltage scaling, leakage power

Laboratory: IRISA/INRIA –CAIRN project-team (Lannion)

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The last years have seen an increasing interest in the development of low-power architectures. Moreover, it is now well admitted that power has become the major constraint for VLSI circuit and system-on-chip (SoC) design. Two main techniques can be used for a significant reduction of energy in CMOS chips: firstly, when considering static power due to current leakage in transistors, power and ground gating [2] – i.e. cutting-off the power supply of a set of transistors – can be used when the gates are not active; and secondly voltage scaling of the power supply [1] (Vdd), together with a chip frequency scaling, gives quadratic (or even more) gains in the dynamic and static power consumption and can still be used while the chip is running. In our group, we are currently tackling power gating in the context of control-intensive applications such as wireless sensor networks, and have shown some substantial gains when compared to classical microprocessor-based architectures [3].

Also, predictions from the silicon industry [4] have shown that the percentage of area and power due to memory in an SoC is continuously increasing, and will reach in the next years up to 90% of the area and thus of the static power. The predominance of the memory is true for most of the SoC application domains (high-performance processors, domain-specific SoC) and is also the case for reconfigurable architectures such as FPGAs. Therefore, reducing the power due to the memory is a major issue and is only achievable with the above-mentioned techniques of power gating and Vdd scaling. Of course, these techniques require architecture- and circuit-level evolutions of the memory structure.

The objective of this Master's thesis is to study how Vdd scaling and gating can be applied to an SRAM memory structure and to characterize the power benefit that these techniques can provide. Also, playing with power supply will have drawbacks on the performance (access time) and the remanence of data that need to be studied in detail.
After a deep literature review, some transistor-level and layout-level design and simulation with CAD tools (SPICE, Cadence Virtuoso) will be performed for this study. The memory structure will be designed for two application domains: a classical embedded SRAM and multiple context memory with different power/voltage/performance trade-offs of a low-power FPGA (and especially an FPGA embedded into an SoC). In case of encouraging results, some prototype chips can moreover be designed and fabricated in the context of an embedded FPGA (eFPGA) proposed in our group for research on dynamic reconfiguration.

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