André Seznec
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Short Biography

André Seznec was born in 1959. He got a Doctorat ès Sciences in computer sciences from University of Rennes I in June 1987. He was hired as a researcher at INRIA Rennes in October 1986. He was promoted as Research Director (DR2) at INRIA in 1994, a Senior Research Director (DR1) in 2002 and a Fellow Research Director (DR0) in 2012.

He has lead the CAPS project-team at INRIA Rennes from 1994 to 2008 and the ALF project-team from 2009 to 2016. He is now a member of the PACAP project-team.

From Feb. 1999 to Feb. 2000, André Seznec spent a sabbatical year with Alpha Development Group at Compaq where he designed the branch predictor of the Alpha EV8.

André Seznec has focused his research on processor architecture since the beginning of his Ph.D. thesis in 1983.

Major research projects

André Seznec initially worked on supercomputer architectures targeting scientific applications. In collaboration with other members of his team, André Seznec has been working on software projects for enabling high performance or architecture simulation. Since 1991, André Seznec main research activity has ported on the architecture of microprocessors, including caches, pipeline, branch predictors, speculative execution, multithreading and multicores.

Architectures for scientific computing

1983-1985, 1991-92 1999-2000: vectors in parallel memories on vector computers
1985-1988: DSPA architecture,
1988-1991: definition and development of the OPAC floating-point coprocessor.

Software environments and compilation for high performance

1998-2000: Calvin2+DICE: an emulation platform on SPARC
1995-1998: SALTO, a System for Assembly Language Transformation and Optimization
1997-2000: GCDS, a Global Constraint Driven Strategy for compilers
1995-1999: Ialloc a data layout optimization library for irregular structure
2002-2006 HAVEGE, software generation of unpredictable random numbers

Microprocessor architecture

1991-..: cache design
2000-..: pipeline structure and organization
1996-..: sequencing, branch prediction, speculative execution
1993-..: simultaneous multithreading and on-chip multiprocessing
2006-..: multicore architecture for high sequential performance

Bibliography record

André Seznec has published more than 30 papers in international journals including IEEE transactions on computers (5), IEEE transaction on parallel and distributed computing, ACM Transactions on Architecture and Code Optimizations (11), Journal on Instruction Level Parallelism (5), Journal of Parallel and Distributed Computing (4), ACM Transaction on Modeling and Computer Simulations, IEEE Micro (2), ACM Transaction on Computer Systems. He has published over 60 papers in international conferences on computer architecture including the five top conferences ISCA (15 papers), Micro (9 papers), ASPLOS, HPCA (9 papers) and PACT (4 papers).

Teaching experience

Since 1993, A. Seznec has been in charge of the lecture on High Performance Architecture in the Master of research in computer science at University of Rennes I.

Past and current Ph. D. students

A. André Seznec has graduated 26 PhD students from 1991 to 2017. Some of these students have joined major microprocessor manufacturers, others have joined startups and academy.

B. André Seznec is currently advising 3 PhD students.

Program committees/Editorial board/Conference organization

A. André Seznec is on the editorial board of IEEE Micro and ACM Transactions on Architecture and Code Optimizations.

B. Since 1996, A. Seznec has been a member of the program committees of most of the major conferences in computer architecture, ACM-IEEE ISCA (8 times), IEEE HPCA (9 times), ACM-IEEE Micro (7 times), IEEE PACT (2 times) and many other international conferences (ICS, Europar, MASCOTT, ISPASS, CASES, Computing Frontiers, ICPP, ICCD, SAMOS,..) and workshops.

C. He has been program co-chair of the ICS conference in 2004, program chair of the parallel architecture workshop at EUROPAR in 2001, program co-chair of the HIPEAC 2013 conference and of the PACT 2013 conference and the program chair of the ACM-IEEE ISCA 2016.

D. André Seznec was the general co-chair of the 4th HiPEAC conference in January 2009 and the general chair of the ISCA symposium in June 2010.

Distinctions

A. André Seznec is member of the hall of fame of the ACM/IEEE ISCA conference (15 papers), IEEE HPCA conference (9 papers) and IEEE Micro (9 papers).

B. André Seznec won the best practice award at the Championship Branch Prediction (CBP) in 2004. He won both the idealistic and realistic track at CBP2 in 2006. He also won both tracks (conditional and indirect) of the CBP3 in 2011, the three tracks of CBP4 in 2014 and the three tracks of CBP5 in 2016.

C. In 2012, André Seznec has received the first Intel Research Impact Medal for his *« exemplary work on high-performance computer micro-architecture, branch prediction and cache architecture"* that *"has been of tremendous benefit to Intel, the industry, and the academic community as a whole"*

D. On January 2013, André Seznec has been elevated as an IEEE fellow *"for contributions to design of branch predictors and cache memory for processor architectures"*

E. On December 2016, André Seznec has been elevated as an ACM fellow *"for contributions to branch prediction and cache memory"*.

Past funding ID

A. Seznec's research has been partially supported by research grants from Intel since 2001 and by an academic award from IBM in 2010. He has been participating to several national research projects in France as well as several EU funded projects. He is a member of the HiPEAC4 network.

In october 2010, André Seznec was awarded an ERC advanced grant, DAL (04-2011,03-2016), for 5 years to work on the microarchitecture on the 2020's processor.

Start-up participation

A. Seznec was one of the co-founders of CAPS Entreprise (2003-2014), a start-up that emerged from the CAPS project-team in 2003. CAPS Entreprise was one of the major actors in compiler environments for GPGPU computing.

Recent international collaborations (from 2010)

Pr David Wood, University of Wisconsin, Pr Andreas Moshovos and Natalie-Enright Jaegger, University of Toronto, Pr Erik Hagersten, Upsala University, Pr Onur Mulu, Carnegie Mellon (now ETH Zurich), Pr Moinuddin Qureshi, Georgia Tech, Pr Yanos Sazeides, University of Cyprus.